

B. E. 2018 Scheme Fifth Semester Syllabus (EC / TC)

Choice Based Credit System (CBCS) and Outcome Based Education (OBE)

SEMESTER – V

TECHNOLOGICAL INNOVATION MANAGEMENT AND ENTREPRENEURSHIP

Course Code	: 18ES51	CIE Marks : 40
Lecture Hours/Week	: 03	SEE Marks : 60
Total Number of Lecture Hours	: 40 (08 Hours / Module)	Exam Hours : 03
CREDITS 03		

Course Learning Objectives: This course will enable students to:

- Understand basic skills of Management
- Understand the need for Entrepreneurs and their skills
- Identify the Management functions and Social responsibilities
- Understand the Ideation Process, creation of Business Model, Feasibility Study and sources of funding

Module-1

Management: Nature and Functions of Management – Importance, Definition, Management Functions, Levels of Management, Roles of Manager, Managerial Skills, Management & Administration, Management as a Science, Art & Profession (**Selected topics of Chapter 1, Text 1**).

Planning: Planning–Nature, Importance, Types, Steps and Limitations of Planning; Decision Making – Meaning, Types and Steps in Decision Making (**Selected topics from Chapters 4 & 5, Text 1**). **L1,L2**

Module-2

Organizing and Staffing: Organization–Meaning, Characteristics, Process of Organizing, Principles of Organizing, Span of Management (meaning and importance only), Departmentalisation, Committees–Meaning, Types of Committees; Centralization Vs Decentralization of Authority and Responsibility; **Staffing**–Need and Importance, Recruitment and Selection Process (**Selected topics from Chapters 7, 8 & 11, Text 1**).

Directing and Controlling: Meaning and Requirements of Effective Direction, Giving Orders; Motivation–Nature of Motivation, Motivation Theories (Maslow’s Need-Hierarchy Theory and Herzberg’s Two Factor Theory); Communication – Meaning, Importance and Purposes of Communication; Leadership–Meaning, Characteristics, Behavioural Approach of Leadership;

Coordination-Meaning, Types, Techniques of Coordination; Controlling – Meaning, Need for Control System, Benefits of Control, Essentials of Effective Control System, Steps in Control Process
(Selected topics from Chapters 15 to 18 and 9, Text 1). L1,L2

Module-3

Social Responsibilities of Business: Meaning of Social Responsibility, Social Responsibilities of Business towards Different Groups, Social Audit, Business Ethics and Corporate Governance (Selected topics from Chapter 3, Text 1).

Entrepreneurship: Definition of Entrepreneur, Importance of Entrepreneurship, concepts of Entrepreneurship, Characteristics of successful Entrepreneur, Classification of Entrepreneurs, Myths of Entrepreneurship, Entrepreneurial Development models, Entrepreneurial development cycle, Problems faced by Entrepreneurs and capacity building for Entrepreneurship (Selected topics from Chapter 2, Text 2). L1,L2

Module-4

Family Business: Role and Importance of Family Business, Contributions of Family Business in India, Stages of Development of a Family Business, Characteristics of a Family-owned Business in India, Various types of family businesses (Selected topics from Chapter 4,(Page 71-75) Text 2).

Idea Generation and Feasibility Analysis- Idea Generation; Creativity and Innovation; Identification of Business Opportunities; Market Entry Strategies; Marketing Feasibility; Financial Feasibilities; Political Feasibilities; Economic Feasibility; Social and Legal Feasibilities; Technical Feasibilities; Managerial Feasibility, Location and Other Utilities Feasibilities.(Selected topics from Chapter 6(Page No. 111-117) & Chapter 7(Page No. 140-142), Text 2)

L1,L2

Module-5

Business model – Meaning, designing, analyzing and improvising; Business Plan – Meaning, Scope and Need; Financial, Marketing, Human Resource and Production/Service Plan; Business plan Formats; Project report preparation and presentation; Why some Business Plan fails? (Selected topics from Chapter 8 (Page No 159-164, Text 2)

Financing and How to start a Business? Financial opportunity identification; Banking sources; Nonbanking Institutions and Agencies; Venture Capital – Meaning and Role in Entrepreneurship; Government Schemes for funding business; Pre launch, Launch and Post launch requirements; Procedure for getting License and Registration; Challenges and Difficulties in Starting an Enterprise(Selected topics from Chapter 7(Page No 147-149), Chapter 5(Page No 93-99) & Chapter 8(Page No. 166-172) Text 2)

Project Design and Network Analysis: Introduction, Importance of Network

Analysis, Origin of PERT and CPM, Network, Network Techniques, Need for Network Techniques, Steps in PERT, CPM, Advantages, Limitations and Differences.

(Selected topics from Chapters 20, Text 3).

L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Understand the fundamental concepts of Management and Entrepreneurship and opportunities in order to setup a business
2. Identify the various organizations' architecture
3. Describe the functions of Managers, Entrepreneurs and their social responsibilities
4. Understand the components in developing a business plan
5. Recognize the various sources of funding and institutions supporting entrepreneurs

Text Books:

1. Principles of Management – P.C Tripathi, P.N Reddy, McGraw Hill Education, 6th Edition, 2017. ISBN-13:978-93-5260-535-4.
2. Entrepreneurship Development Small Business Enterprises- Poornima M Charantimath, Pearson Education 2008, ISBN 978-81-7758-260-4.
3. Dynamics of Entrepreneurial Development and Management by Vasant Desai. HPH 2007, ISBN: 978-81-8488-801-2.
4. Robert D. Hisrich, Mathew J. Manimala, Michael P Peters and Dean A. Shepherd, “Entrepreneurship”, 8th Edition, Tata Mc-Graw Hill Publishing Co.Ltd.- New Delhi, 2012

Reference Book:

1. Essentials of Management: An International, Innovation and Leadership perspective by Harold Koontz, Heinz Weihrich McGraw Hill Education, 10th Edition 2016. ISBN- 978-93-392-2286-4.

DIGITAL SIGNAL PROCESSING

Course Code	: 18EC52	CIE Marks : 40
Lecture Hours/Week	: 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours	: 50 (10 Hrs / Module)	Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to

- Understand the frequency domain sampling and reconstruction of discrete time signals.
- Study the properties and the development of efficient algorithms for the computation of DFT.
- Realization of FIR and IIR filters in different structural forms.
- Learn the procedures to design of IIR filters from the analog filters using impulse invariance and bilinear transformation.
- Study the different windows used in the design of FIR filters and design appropriate filters based on the specifications.
- Understand the architecture and working of DSP processor

Module-1

Discrete Fourier Transforms (DFT): Frequency domain sampling and Reconstruction of Discrete Time Signals, The Discrete Fourier Transform, DFT as a linear transformation, Properties of the DFT: Periodicity, Linearity and Symmetry properties, Multiplication of two DFTs and Circular Convolution, Additional DFT properties.

[Text 1],

L1,L2,L3

Module-2

Linear filtering methods based on the DFT: Use of DFT in Linear Filtering, Filtering of Long data Sequences.

Fast-Fourier-Transform (FFT) algorithms: Efficient Computation of the DFT: Radix-2 FFT algorithms for the computation of DFT and IDFT—decimation-in-time and decimation-in-frequency algorithms.

[Text 1],

L1,L2, L3

Module-3

Design of FIR Filters: Characteristics of practical frequency–selective filters, Symmetric and Antisymmetric FIR filters, Design of Linear-phase FIR filters using windows - Rectangular, Hamming, Hanning, Bartlett windows. Design of FIR filters using frequency sampling method. Structure for FIR Systems: Direct form, Cascade form and Lattice structures.

[Text1],

L1, L2, L3

Module-4

IIR Filter Design: Infinite Impulse response Filter Format, Bilinear Transformation Design Method, Analog Filters using Lowpass prototype transformation, Normalized Butterworth Functions, Bilinear Transformation and Frequency Warping, Bilinear Transformation Design Procedure, Digital Butterworth Filter Design using BLT. Realization of IIR Filters in Direct form I and II.

[Text 2],

L1,L2,L3

Module-5

Digital Signal Processors: DSP Architecture, DSP Hardware Units, Fixed point format, Floating point Format, IEEE Floating point formats, Fixed point digital signal processors, Floating point processors, FIR and IIR filter implementations in Fixed point systems.

[Text 2],

L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

1. Determine response of LTI systems using time domain and DFT techniques.
2. Compute DFT of real and complex discrete time signals.
3. Compute DFT using FFT algorithms and linear filtering approach.
4. Design and realize FIR and IIR digital filters.
5. Understand the DSP processor architecture.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60

Text Book:

1. Proakis & Manolakis, “Digital Signal Processing – Principles Algorithms & Applications”, 4th Edition, Pearson education, New Delhi, 2007. ISBN: 81-317-1000-9.
2. Li Tan, Jean Jiang, “Digital Signal processing – Fundamentals and Applications”, Academic Press, 2013, ISBN: 978-0-12-415893.

Reference Books:

1. Sanjit K Mitra, "Digital Signal Processing, A Computer Based Approach", 4th Edition, McGraw Hill Education, 2013,
2. Oppenheim & Schaffer, "Discrete Time Signal Processing" , PHI, 2003.
3. D.Ganesh Rao and Vineeth P Gejji, "Digital Signal Processing" Cengage India Private Limited, 2017, ISBN: 9386858231

PRINCIPLES OF COMMUNICATION SYSTEMS

Course Code	: 18EC53	CIE Marks : 40
Lecture Hours/Week	: 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours	: 50 (10 Hrs / Module)	Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to

- Understand and analyse concepts of Analog Modulation schemes viz; AM, FM, Low pass sampling and Quantization as a random process.
- Understand and analyse concepts digitization of signals viz; sampling, quantizing and encoding.
- Evolve the concept of SNR in the presence of channel induced noise and study Demodulation of analog modulated signals.
- Evolve the concept of quantization noise for sampled and encoded signals and study the concepts of reconstruction from these samples at a receiver.

Module-1

AMPLITUDE MODULATION: Introduction, Amplitude Modulation: Time & Frequency Domain description, Switching modulator, Envelop detector. **(3.1 – 3.2 in Text)**

DOUBLE SIDE BAND-SUPPRESSED CARRIER MODULATION: Time and Frequency Domain description, Ring modulator, Coherent detection, Costas Receiver, Quadrature Carrier Multiplexing. **(3.3 – 3.4 in Text)**

SINGLE SIDE-BAND AND VESTIGIAL SIDEBAND METHODS OF MODULATION: SSB Modulation, VSB Modulation, Frequency Translation, Frequency- Division Multiplexing, Theme Example: VSB Transmission of Analog and Digital Television. **(3.5 – 3.8 in Text)**

L1, L2, L3

Module-2

ANGLE MODULATION: Basic definitions, Frequency Modulation: Narrow Band FM, Wide Band FM, Transmission bandwidth of FM Signals, Generation of FM Signals, Demodulation of FM Signals, FM Stereo Multiplexing, Phase-Locked Loop: Nonlinear model of PLL, Linear model of PLL, Nonlinear Effects in FM Systems. The Superheterodyne Receiver **(4.1 – 4.6 of Text)**

L1, L2, L3

Module-3

[Review of Mean, Correlation and Covariance functions of Random Processes. (No questions to be set on these topics)]

NOISE - Shot Noise, Thermal noise, White Noise, Noise Equivalent Bandwidth **(5.10 in Text)**

NOISE IN ANALOG MODULATION: Introduction, Receiver Model, Noise in DSB-SC receivers. Noise in AM receivers, Threshold effect, Noise in FM receivers, Capture effect, FM threshold effect, FM threshold reduction, Pre-emphasis and De-emphasis in FM **(6.1 – 6.6 in Text)**

L1,L2,L3

Module-4

SAMPLING AND QUANTIZATION: Introduction, Why Digitize Analog Sources?, The Low pass Sampling process Pulse Amplitude Modulation. Time Division Multiplexing, Pulse-Position Modulation, Generation of PPM Waves, Detection of PPM Waves. **(7.1 – 7.7 in Text)**

L1,L2,L3

Module-5

SAMPLING AND QUANTIZATION (Contd): The Quantization Random Process, Quantization Noise, Pulse–Code Modulation: Sampling, Quantization, Encoding, Regeneration, Decoding, Filtering, Multiplexing; Delta Modulation **(7.8 – 7.10 in Text)**,

Application examples - (a) Video + MPEG **(7.11 in Text)** and (b) Vocoders **(refer Section 6.8 of Reference Book 1)**.

L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Analyze and compute performance of AM and FM modulation in the presence of noise at the receiver.
2. Analyze and compute performance of digital formatting processes with quantization noise.
3. Multiplex digitally formatted signals at Transmitter.
4. Demultiplex the signals and reconstruct digitally formatted signals at the receiver.
5. Design /Demonstrate the use of digital formatting in Multiplexers, Vocoders and Video transmission.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.

- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. “Communication Systems”, Simon Haykin & Moher, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN 978 – 81 – 265 – 2151 – 7.

Reference Books:

1. Modern Digital and Analog Communication Systems, B. P. Lathi, Oxford University Press, 4th edition.
2. An Introduction to Analog and Digital Communication, Simon Haykin, John Wiley India Pvt. Ltd., 2008, ISBN 978–81–265–3653–5.
3. Principles of Communication Systems, H. Taub & D.L.Schilling, TMH, 2011.
4. Communication Systems, Harold P.E, Samy A. Mahmoud, Lee Elliott Stern, Pearson Edition, 2004.

INFORMATION THEORY and CODING

Course Code	: 18EC54	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (8 Hrs / Module)	Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to

- Understand the concept of Entropy, Rate of information and order of the source with reference to dependent and independent source.
- Study various source encoding algorithms.
- Model discrete & continuous communication channels.
- Study various error control coding algorithms.

Module-1

Information Theory: Introduction, Measure of information, Information content of message, Average Information content of symbols in Long Independent sequences, Average Information content of symbols in Long dependent sequences, Markov Statistical Model for Information Sources, Entropy and Information rate of Markoff Sources

(Section 4.1, 4.2 of Text 1)

L1, L2, L3

Module-2

Source Coding: Encoding of the Source Output, Shannon's Encoding Algorithm (Sections 4.3, 4.3.1 of Text 1), Shannon Fano Encoding Algorithm (Section 2.15 of Reference Book 4)

Source coding theorem, Prefix Codes, Kraft McMillan Inequality property – KMI, Huffman codes (Section 2.2 of Text 2)

L1, L2, L3

Module-3

Information Channels: Communication Channels, Discrete Communication channels Channel Matrix, Joint probability Matrix, Binary Symmetric Channel, System Entropies. (Section 4.4, 4.5, 4.5.1, 4.5.2 of Text 1)

Mutual Information, Channel Capacity, Channel Capacity of Binary Symmetric Channel, (Section 2.5, 2.6 of Text 2)

Binary Erasure Channel, Muroga's Theorem (Section 2.27, 2.28 of Reference Book 4)

L1, L2, L3

Module-4

Error Control Coding:

Introduction, Examples of Error control coding, methods of Controlling Errors, Types of Errors, types of Codes, Linear Block Codes: matrix description of Linear Block Codes, Error detection & Correction capabilities of Linear Block Codes, Single error correction Hamming code, Table lookup Decoding using Standard Array.

Binary Cyclic Codes: Algebraic Structure of Cyclic Codes, Encoding using an $(n-k)$ Bit Shift register, Syndrome Calculation, Error Detection and Correction (Sections 9.1, 9.2, 9.3, 9.3.1, 9.3.2, 9.3.3 of Text 1),

L1, L2, L3

Module-5

Convolution Codes: Convolution Encoder, Time domain approach, Transform domain approach, Code Tree, Trellis and State Diagram, The Viterbi Algorithm) (Section 8.5 – Articles 1, 2 and 3, 8.6- Article 1 of Text 2),

L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

1. Explain concept of Dependent & Independent Source, measure of information, Entropy, Rate of Information and Order of a source
2. Represent the information using Shannon Encoding, Shannon Fano, Prefix and Huffman Encoding Algorithms
3. Model the continuous and discrete communication channels using input, output and joint probabilities
4. Determine a codeword comprising of the check bits computed using Linear Block codes, cyclic codes & convolutional codes
5. Design the encoding and decoding circuits for Linear Block codes, cyclic codes, convolutional codes, BCH and Golay codes.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Digital and Analog Communication Systems, K. Sam Shanmugam, John Wiley India Pvt. Ltd, 1996.
2. Digital Communication, Simon Haykin, John Wiley India Pvt. Ltd, 2008.

Reference Books:

1. ITC and Cryptography, Ranjan Bose, TMH, II edition, 2007
2. Principles of Digital Communication, J. Das, S. K. Mullick, P. K. Chatterjee, Wiley, 1986 - Technology & Engineering
3. Digital Communications – Fundamentals and Applications, Bernard Sklar, Second Edition, Pearson Education, 2016, ISBN: 9780134724058.
4. Information Theory and Coding, HariBhat, Ganesh Rao, Cengage, 2017.
5. Error Correction Coding, Todd K Moon, Wiley Std. Edition, 2006

ELECTROMAGNETIC WAVES

Course Code	: 18EC55	CIE Marks	: 40
Lecture Hours/Week	: 3	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (8 Hrs / Module)	Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Study the different coordinate systems, Physical significance of Divergence, Curl and Gradient.
- Understand the applications of Coulomb's law and Gauss law to different charge distributions and the applications of Laplace's and Poisson's Equations to solve real time problems on capacitance of different charge distributions.
- Understand the physical significance of Biot-Savart's, Ampere's Law and Stokes' theorem for different current distributions.
- Infer the effects of magnetic forces, materials and inductance.
- Know the physical interpretation of Maxwell's equations and applications for Plane waves for their behavior in different media.
- Acquire knowledge of Poynting theorem and its application of power flow.

Module-1

Revision of Vector Calculus – (Text 1: Chapter 1)

Coulomb's Law, Electric Field Intensity and Flux density: Experimental law of Coulomb, Electric field intensity, Field due to continuous volume charge distribution, Field of a line charge, Field due to Sheet of charge, Electric flux density, Numerical Problems. (Text: Chapter 2.1 to 2.5, 3.1)

L1, L2, L3

Module-2

Gauss's law and Divergence: Gauss law, Application of Gauss law to point charge, line charge, Surface charge and volume charge, Point (differential) form of Gauss law, Divergence. Maxwell's First equation (Electrostatics), Vector Operator ∇ and divergence theorem, Numerical Problems (Text: Chapter 3.2 to 3.7).

Energy, Potential and Conductors: Energy expended or work done in moving a point charge in an electric field, The line integral, Definition of potential difference and potential, The potential field of point charge, Potential gradient, Numerical Problems (Text: Chapter 4.1 to 4.4 and 4.6). Current and Current density, Continuity of current. (Text: Chapter 5.1, 5.2)

L1, L2, L3

Module-3

Poisson's and Laplace's Equations: Derivation of Poisson's and Laplace's Equations, Uniqueness theorem, Examples of the solution of Laplace's equation, Numerical problems on Laplace equation (**Text: Chapter 7.1 to 7.3**)

Steady Magnetic Field: Biot-Savart Law, Ampere's circuital law, Curl, Stokes' theorem, Magnetic flux and magnetic flux density, Basic concepts Scalar and Vector Magnetic Potentials, Numerical problems. (**Text: Chapter 8.1 to 8.6**)

L1, L2, L3

Module-4

Magnetic Forces: Force on a moving charge, differential current elements, Force between differential current elements, Numerical problems (**Text: Chapter 9.1 to 9.3**).

Magnetic Materials: Magnetization and permeability, Magnetic boundary conditions, The magnetic circuit, Potential energy and forces on magnetic materials, Inductance and mutual reactance, Numerical problems (**Text: Chapter 9.6 to 9.7**).

Faraday' law of Electromagnetic Induction –Integral form and Point form, Numerical problems (**Text: Chapter 10.1**)

L1, L2, L3

Module-5

Maxwell's equations Continuity equation, Inconsistency of Ampere's law with continuity equation, displacement current, Conduction current, Derivation of Maxwell's equations in point form, and integral form, Maxwell's equations for different media, Numerical problems (**Text: Chapter 10.2 to 10.4**)

Uniform Plane Wave: Plane wave, Uniform plane wave, Derivation of plane wave equations from Maxwell's equations, Solution of wave equation for perfect dielectric, Relation between E and H, Wave propagation in free space, Solution of wave equation for sinusoidal excitation, wave propagation in any conducting media (γ , α , β , η) and good conductors, Skin effect or Depth of penetration, Poynting's theorem and wave power, Numerical problems. (**Text: Chapter 12.1 to 12.4**)

L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

1. Evaluate problems on electrostatic force, electric field due to point, linear, volume charges by applying conventional methods and charge in a volume.
2. Apply Gauss law to evaluate Electric fields due to different charge distributions and Volume Charge distribution by using Divergence Theorem.

3. Determine potential and energy with respect to point charge and capacitance using Laplace equation and Apply Biot-Savart's and Ampere's laws for evaluating Magnetic field for different current configurations
4. Calculate magnetic force, potential energy and Magnetization with respect to magnetic materials and voltage induced in electric circuits.
5. Apply Maxwell's equations for time varying fields, EM waves in free space and conductors and Evaluate power associated with EM waves using Poynting theorem

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. W.H. Hayt and J.A. Buck, —Engineering Electromagnetics, 8th Edition, Tata McGraw-Hill, 2014, ISBN-978-93-392-0327-6.

Reference Books:

1. Elements of Electromagnetics – Matthew N.O., Sadiku, Oxford university press, 4th Edn.
2. Electromagnetic Waves and Radiating systems – E. C. Jordan and K.G. Balmain, PHI, 2nd Edn.
3. Electromagnetics- Joseph Edminister, Schaum Outline Series, McGraw Hill.
4. Fundamentals of Electromagnetics for Engineering - N. Narayana Rao, Pearson.

Verilog HDL

Course Code	: 18EC56	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (08 Hrs/Module)	Exam Hours	: 03
CREDITS–03			

Course Learning Objectives: This course will enable students to:

- Learn different Verilog HDL constructs.
- Familiarize the different levels of abstraction in Verilog.
- Understand Verilog Tasks, Functions and Directives.
- Understand timing and delay Simulation.
- Understand the concept of logic synthesis and its impact in verification

Module 1

Overview of Digital Design with Verilog HDL: Evolution of CAD, emergence of HDLs, typical HDL-flow, why Verilog HDL?, trends in HDLs.

Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block. **L1,L2,L3**

Module 2

Basic Concepts: Lexical conventions, data types, system tasks, compiler directives.

Modules and Ports: Module definition, port declaration, connecting ports, hierarchical name referencing **L1,L2,L3**

Module 3

Gate-Level Modeling: Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays.

Dataflow Modeling: Continuous assignments, delay specification, expressions, operators, operands, operator types. **L1,L2,L3**

Module 4

Behavioral Modeling: Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks.

Tasks and Functions: Differences between tasks and functions, declaration, invocation, automatic tasks and functions. **L1,L2,L3**

Module 5

Useful Modeling Techniques: Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks.

Logic Synthesis with Verilog: Logic Synthesis, Impact of logic synthesis, Verilog HDL Synthesis, Synthesis design flow, Verification of Gate-Level Netlist. (**Chapter 14 till 14.5 of Text**).
L1,L2,L3

Course Outcomes: At the end of this course, students will be able to

1. Write Verilog programs in gate, dataflow (RTL), behavioral and switch modeling levels of Abstraction.
2. Design and verify the functionality of digital circuit/system using test benches.
3. Identify the suitable Abstraction level for a particular digital design.
4. Write the programs more effectively using Verilog tasks, functions and directives.
5. Perform timing and delay Simulation and Interpret the various constructs in logic synthesis.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Samir Palnitkar, “**Verilog HDL: A Guide to Digital Design and Synthesis**”, Pearson Education, Second Edition.

Reference Books:

1. Donald E. Thomas, Philip R. Moorby, “The Verilog Hardware Description Language”, Springer Science+Business Media, LLC, Fifth edition.
2. Michael D. Ciletti, “Advanced Digital Design with the Verilog HDL” Pearson (Prentice Hall), Second edition.
3. Padmanabhan, Tripura Sundari, “Design through Verilog HDL”, Wiley, 2016 or earlier.

DIGITAL SIGNAL PROCESSING LABORATORY

Course Code : 18ECL57	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to

- Simulate discrete time signals and verification of sampling theorem.
- Compute the DFT for a discrete signal and verification of its properties using MATLAB.
- Find solution to the difference equations and computation of convolution and correlation along with the verification of properties.
- Compute and display the filtering operations and compare with the theoretical values.
- Implement the DSP computations on DSP hardware and verify the result.

Laboratory Experiments

Following Experiments to be done using MATLAB / SCILAB / OCTAVE or equivalent:

1. Verification of sampling theorem (use interpolation function).
2. Linear and circular convolution of two given sequences, Commutative, distributive and associative property of convolution.
3. Auto and cross correlation of two sequences and verification of their properties
4. Solving a given difference equation.
5. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum (using DFT equation and verify it by built-in routine).
6. (i) Verification of DFT properties (like Linearity and Parseval's theorem, etc.)
(ii) DFT computation of square pulse and Sinc function etc.

7. Design and implementation of Low pass and High pass FIR filter to meet the desired specifications (using different window techniques) and test the filter with an audio file. Plot the spectrum of audio signal before and after filtering.
8. Design and implementation of a digital IIR filter (Low pass and High pass) to meet given specifications and test with an audio file. Plot the spectrum of audio signal before and after filtering.

Following Experiments to be done using DSP kit

9. Obtain the Linear convolution of two sequences.
10. Compute Circular convolution of two sequences.
11. Compute the N-point DFT of a given sequence.
12. Determine the Impulse response of first order and second order system.
13. Generation of sine wave and standard test signals

Course Outcomes:

On the completion of this laboratory course, the students will be able to:

1. Understand the concepts of analog to digital conversion of signals and frequency domain sampling of signals.
2. Model the discrete time signals and systems and verify its properties and results.
3. Implement discrete computations using DSP processor and verify the results.
4. Realize the digital filters using a simulation tool and analyze the response of the filter for an audio signal.
5. Write programs using Matlab / Scilab/Octave to illustrate DSP concepts.

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
3. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Reference Books:

1. Vinay K Ingle, John G Proakis, Digital Signal Processing using MATLAB, Fourth Edition, Cengage India Private Limited, 2017.

HDL LABORATORY

Course Code : 18ECL58	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to:

- Familiarize with the CAD tool to write HDL programs.
- Understand simulation and synthesis of digital design.
- Program FPGAs/CPLDs to synthesize the digital designs.
- Interface hardware to programmable ICs through I/O ports.
- Choose either Verilog or VHDL for a given Abstraction level.

Note: Programming can be done using any compiler. Download the programs on a FPGA/CPLD board and performance testing may be done using 32 channel pattern generator and logic analyzer apart from verification by simulation with tools such as Altera/Modelsim or equivalent.

PART A

1. Write Verilog program for the following combinational design along with test bench to verify the design:
 - a. 2 to 4 decoder realization using NAND gates only (structural model)
 - b. 8 to 3 encoder with priority and without priority (behavioural model)
 - c. 8 to 1 multiplexer using case statement and if statements
 - d. 4-bit binary to gray converter using 1-bit gray to binary converter 1-bit adder and subtractor
2. Model in Verilog for a full adder and add functionality to perform logical operations of XOR, XNOR, AND and OR gates. Write test bench with appropriate input patterns to verify the modeled behaviour.
3. Verilog 32-bit ALU shown in figure below and verify the functionality of ALU by selecting appropriate test patterns. The functionality of the ALU is presented in Table 1.
 - a. Write test bench to verify the functionality of the ALU considering all possible input patterns
 - b. The enable signal will set the output to required functions if enabled, if disabled all the outputs are set to tri-state
 - c. The acknowledge signal is set high after every operation is complete

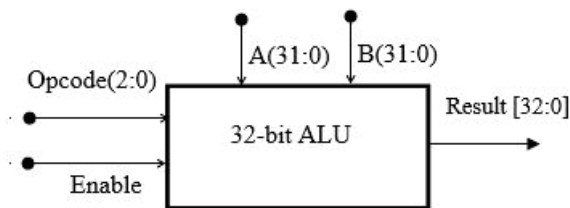


Figure 1 ALU top level block diagram

Table 1 ALU Functions

Opcode (2:0)	ALU Operation	Remarks	
000	A + B	Addition of two numbers	Both A and B are in two's complement format
001	A - B	Subtraction of two numbers	
010	A + 1	Increment Accumulator by 1	A is in two's complement format
011	A - 1	Decrement accumulator by 1	
100	A	True	Inputs can be in any format
101	A Complement	Complement	
110	A OR B	Logical OR	
111	A AND B	Logical AND	

4. Write Verilog code for SR, D and JK and verify the flip flop.
5. Write Verilog code for 4-bit BCD synchronous counter.
6. Write Verilog code for counter with given input clock and check whether it works as clock divider performing division of clock by 2, 4, 8 and 16. Verify the functionality of the code.

PART-B

Interfacing and Debugging (EDWinXP, PSpice, MultiSim, Proteus, CircuitLab or any other equivalent tool can be used)

1. Write a Verilog code to design a clock divider circuit that generates 1/2, 1/3rd and 1/4th clock from a given input clock. Port the design to FPGA and validate the functionality through oscilloscope.
2. Interface a DC motor to FPGA and write Verilog code to change its speed and direction.
3. Interface a Stepper motor to FPGA and write Verilog code to control the Stepper motor rotation which in turn may control a Robotic Arm. External switches to be used for different controls like rotate the Stepper motor
 (i) +N steps if Switch no.1 of a Dip switch is closed (ii) +N/2 steps if Switch no. 2 of a Dip switch is closed (iii) -N steps if Switch no. 3 of a Dip switch is closed etc.

4. Interface a DAC to FPGA and write Verilog code to generate Sine wave of frequency F KHz (eg. 200 KHz) frequency. Modify the code to down sample the frequency to $F/2$ KHz. Display the Original and Down sampled signals by connecting them to an oscilloscope.
5. Write Verilog code using FSM to simulate elevator operation.
6. Write Verilog code to convert an analog input of a sensor to digital form and to display the same on a suitable display like set of simple LEDs, 7-segment display digits or LCD display.

Course Outcomes: At the end of this course, students will be able to:

1. Write the Verilog/VHDL programs to simulate Combinational circuits in Dataflow, Behavioral and Gate level Abstractions.
2. Describe sequential circuits like flip flops and counters in Behavioral description and obtain simulation waveforms.
3. Use FPGA/CPLD kits for down loading Verilog codes and check output.
4. Synthesize Combinational and Sequential circuits on programmable ICs and test the hardware.
5. Interface the hardware to the programmable chips and obtain the required output

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

ENVIRONMENTAL STUDIES

Course Code	:18CIV59	CIE Marks	: 40
Lecture Hours / Week (L:T:P)	:(1:0:0)	SEE Marks	: 60
Credits	:01	Exam Hours	: 02

Module - 1

Ecosystems (Structure and Function): Forest, Desert, Wetlands, Riverine, Oceanic and Lake.

Biodiversity: Types, Value; Hot-spots; Threats and Conservation of biodiversity, Forest Wealth, and Deforestation.

Module - 2

Advances in Energy Systems (Merits, Demerits, Global Status and Applications): Hydrogen, Solar, OTEC, Tidal and Wind.

Natural Resource Management (Concept and case-studies): Disaster Management, Sustainable Mining, Cloud Seeding, and Carbon Trading.

Module - 3

Environmental Pollution (Sources, Impacts, Corrective and Preventive measures, Relevant Environmental Acts, Case-studies): Surface and Ground Water Pollution; Noise pollution; Soil Pollution and Air Pollution.

Waste Management & Public Health Aspects: Bio-medical Wastes; Solid waste; Hazardous wastes; E-wastes; Industrial and Municipal Sludge.

Module - 4

Global Environmental Concerns(Concept, policies and case-studies):Ground water depletion/recharging, Climate Change; Acid Rain; Ozone Depletion; Radon and Fluoride problem in drinking water; Resettlement and rehabilitation of people, Environmental Toxicology.

Module - 5

Latest Developments in Environmental Pollution Mitigation Tools (Concept and Applications): G.I.S. & Remote Sensing, Environment Impact Assessment, Environmental Management Systems, ISO14001; Environmental Stewardship- NGOs.

Field work: Visit to an Environmental Engineering Laboratory or Green Building or Water Treatment Plant or Waste water treatment Plant; ought to be Followed by understanding of process and its brief documentation.

Course outcomes: At the end of the course, students will be able to:

1. Understand the principles of ecology and environmental issues that apply to air, land, and water issues on a global scale.
2. Develop critical thinking and/or observation skills, and apply them to the analysis of a problem or question related to the environment.
3. Demonstrate ecology knowledge of a complex relationship between biotic and a biotic components.
4. Apply their ecological knowledge to illustrate and graph a problem and describe the realities that managers face when dealing with complex issues.
5. Relate to the latest Developments in Environmental Pollution Mitigation Tools.

Question paper pattern:

- The Question paper will have 100 objective questions.
- Each question will be for 01 marks
- Student will have to answer all the questions in an OMR Sheet.
- The Duration of Exam will be 2 hours.

Textbook/s

1. Environmental Studies, Benny Joseph, Tata McGraw – Hill., 2nd Edition, 2012
2. Environmental Studies, S M Prakash, Pristine Publishing House, Mangalore, 3rd Edition- 2018
3. Environmental Studies – From Crisis to Cure, R Rajagopalan, Oxford Publisher, 2005

Reference Books

1. Principles of Environmental Science and Engineering, Raman Sivakumar, Cengage learning, Singapur. 2nd Edition, 2005
2. Environmental Science – working with the Earth, G.Tyler Miller Jr., Thomson Brooks /Cole, 11th Edition, 2006
3. Text Book of Environmental and Ecology, Pratiba Sing, Anoop Singh & Piyush Malaviya, Acme Learning Pvt. Ltd. New Delhi, 1st Edition

B. E. 2018 Scheme Sixth Semester Syllabus (EC)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)

SEMESTER – VI
DIGITAL COMMUNICATION

Course Code	: 18EC61	CIE Marks : 40
Lecture Hours/Week	: 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours	: 50 (10 Hrs / Module)	Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to:

- Understand the mathematical representation of signal, symbol, and noise.
- Understand the concept of signal processing of digital data and signal conversion to symbols at the transmitter and receiver.
- Compute performance metrics and parameters for symbol processing and recovery in ideal and corrupted channel conditions.
- Compute performance parameters and mitigate channel induced impediments in corrupted channel conditions.

Module-1

Bandpass Signal to Equivalent Low pass: Hilbert Transform, Pre-envelopes, Complex envelopes, Canonical representation of bandpass signals, Complex low pass representation of bandpass systems, Complex representation of band pass signals and systems (**Text 1: 2.8, 2.9, 2.10, 2.11, 2.12, 2.13**).

Line codes: Unipolar, Polar, Bipolar (AMI) and Manchester code and their power spectral densities (**Text 1: Ch 6.10**).
Overview of HDB3, B3ZS, B6ZS (**Ref. 1: 7.2**)

L1,L2,L3

Module-2

Signaling over AWGN Channels- Introduction, Geometric representation of signals, Gram-Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel into a vector channel, Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver (**Text 1: 7.1, 7.2, 7.3, 7.4**).

L1,L2,L3

Module – 3

Digital Modulation Techniques: Phase shift Keying techniques using coherent detection: generation, detection and error probabilities of BPSK and QPSK, M-ary PSK, M-ary QAM (**Relevant topics in Text 1 of 7.6, 7.7**).

Frequency shift keying techniques using Coherent detection: BFSK generation, detection and error probability (**Relevant topics in Text 1 of 7.8**).

Non coherent orthogonal modulation techniques: BFSK, DPSK Symbol representation, Block diagrams treatment of Transmitter and Receiver, Probability of error (without derivation of probability of error equation) (**Text 1: 7.11, 7.12, 7.13**).

L1,L2,L3

Module-4

Communication through Band Limited Channels: Digital Transmission through Band limited channels: Digital PAM Transmission through Band limited Channels, Signal design for Band limited Channels: Design of band limited signals for zero ISI–The Nyquist Criterion (statement only), Design of band limited signals with controlled ISI–Partial Response signals, Probability of error for detection of Digital PAM: Probability of error for detection of Digital PAM with Zero ISI, Symbol–by–Symbol detection of data with controlled ISI (**Text 2: 9.1, 9.2, 9.3.1, 9.3.2**).

Channel Equalization: Linear Equalizers (ZFE, MMSE), (**Text 2: 9.4.2**).

L1,L2,L3

Module-5

Principles of Spread Spectrum: Spread Spectrum Communication Systems: Model of a Spread Spectrum Digital Communication System, Direct Sequence Spread Spectrum Systems, Effect of De-spreading on a narrowband Interference, Probability of error (statement only), Some applications of DS Spread Spectrum Signals, Generation of PN Sequences, Frequency Hopped Spread Spectrum, CDMA based on IS-95 (**Text 2: 11.3.1, 11.3.2, 11.3.3, 11.3.4, 11.3.5, 11.4.2**).

L1,L2,L3

Course Outcomes: At the end of the course, the students will be able to:

1. Associate and apply the concepts of Bandpass sampling to well specified signals and channels.
2. Analyze and compute performance parameters and transfer rates for low pass and bandpass symbol under ideal and corrupted non band limited channels.
3. Test and validate symbol processing and performance parameters at the receiver under ideal and corrupted bandlimited channels.

4. Demonstrate that bandpass signals subjected to corruption and distortion in a bandlimited channel can be processed at the receiver to meet specified performance criteria.
5. Understand the principles of spread spectrum communications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Simon Haykin, “Digital Communication Systems”, John Wiley & sons, First Edition, 2014, ISBN 978-0-471-64735-5.
2. John G Proakis and Masoud Salehi, “Fundamentals of Communication Systems”, 2014 Edition, Pearson Education, ISBN 978-8-131-70573-5.

Reference Books:

1. B.P.Lathi and Zhi Ding, “Modern Digital and Analog communication Systems”, Oxford University Press, 4th Edition, 2010, ISBN: 978-0-198-07380-2.
2. Ian A Glover and Peter M Grant, “Digital Communications”, Pearson Education, Third Edition, 2010, ISBN 978-0-273-71830-7.
3. Bernard Sklar and Ray, “Digital Communications - Fundamentals and Applications”, Pearson Education, Third Edition, 2014, ISBN: 978-81-317-2092-9.

EMBEDDED SYSTEMS

Course Code	: 18EC62	CIE Marks : 40
Lecture Hours/Week	: 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours	: 50 (10 Hrs / Module)	Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to:

- Explain the architectural features and instructions of 32 bit microcontroller -ARM Cortex M3.
- Develop Programs using the various instructions of ARM Cortex M3 and C language for different applications.
- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Develop the hardware software co-design and firmware design approaches.
- Explain the need of real time operating system for embedded system applications.

Module 1

ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, Debugging support, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (**Text 1: Ch-1, 2, 3**)

L1,L2

Module 2

ARM Cortex M3 Instruction Sets and Programming: Assembly basics, Instruction list and description, Thumb and ARM instructions, Special instructions, Useful instructions, CMSIS, Assembly and C language Programming (**Text 1: Ch-4, Ch-10.1 to 10.6**)

L1,L2,L3

Module 3

Embedded System Components: Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of ES. Elements of an Embedded System (Block diagram and explanation), Differences between RISC and CISC, Harvard and Princeton, Big and Little Endian formats, Memory (ROM and RAM types), Sensors, Actuators, Optocoupler, Communication Interfaces (I2C, SPI, IrDA, Bluetooth, Wi-Fi, Zigbee only)

(Text 2: All the Topics from Ch-1 and Ch-2 (Fig and explanation before 2.1) 2.1.1.6 to 2.1.1.8, 2.2 to 2.2.2.3, 2.3 to 2.3.2, 2.3.3.3, selected topics of 2.4.1 and 2.4.2 only).

L1, L2

Module 4

Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modeling (excluding UML), Embedded firmware design and development (excluding C language). **Text 2: Ch-3, Ch-4 (4.1, 4.2.1 and 4.2.2 only), Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)**

L1, L2, L3

Module 5

RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques (**Text 2: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2, 10.7, 10.8.1.1, 10.8.1.2, 10.8.2.2, 10.10 only), Ch-12, Ch-13 (a block diagram before 13.1, 13.3, 13.4, 13.5, 13.6 only)**)

L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

1. Describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.
2. Apply the knowledge gained for Programming ARM Cortex M3 for different applications.
3. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
4. Develop the hardware software co-design and firmware design approaches.
5. Explain the need of real time operating system for embedded system applications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", 2nd Edition, Newnes, (Elsevier), 2010.
2. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2nd Edition.

Reference Books:

1. James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008, ISBN: 978-0-471-72180-2.
2. Yifeng Zhu, "Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language and C", 2nd Ed. Man Press LLC ©2015 ISBN: 0982692633 9780982692639.
3. K.V. K. K Prasad, Embedded Real Time Systems, Dreamtech publications, 2003.
4. Rajkamal, Embedded Systems, 2nd Edition, McGraw hill Publications, 2010.

MICROWAVE and ANTENNAS

Course Code	: 18EC63	CIE Marks : 40
Lecture Hours/Week	: 03 + 2 (Tutorial)	SEE marks : 60
Total Number of Lecture Hours	: 50 (10 Hrs / Module)	Exam Hours : 03
CREDITS : 04		

Course Learning Objectives: This course will enable students to:

- Describe the microwave properties and its transmission media
- Describe microwave devices for several applications
- Understand the basics of antenna theory
- Select antennas for specific applications

Module 1

Microwave Tubes: Introduction, Reflex Klystron Oscillator, Mechanism of Oscillations, Modes of Oscillations, Mode Curve (Qualitative Analysis only).
(Text 1: 9.1, 9.2.1)

Microwave Transmission Lines: Microwave Frequencies, Microwave devices, Microwave Systems, Transmission Line equations and solutions, Reflection Coefficient and Transmission Coefficient, Standing Wave and Standing Wave Ratio, Smith Chart, Single Stub matching.

(Text 2: 0.1, 0.2, 0.3, 3.1, 3.2, 3.3, 3.5, 3.6 Except Double stub matching)

L1,L2

Module 2

Microwave Network theory: Introduction, Symmetrical Z and Y-Parameters for reciprocal Networks, S matrix representation of Multi-Port Networks. (Text1: 6.1, 6.2, 6.3)

Microwave Passive Devices: Coaxial Connectors and Adapters, Attenuators, Phase Shifters, Waveguide Tees, Magic tees.

(Text 1: 6.4.2,6.4.14, 6.4.15, 6.4.16)

L1,L2

Module 3

Strip Lines: Introduction, Micro Strip lines, Parallel Strip lines, Coplanar Strip lines, Shielded Strip Lines. (Text 2: 11.1, 11.2, 11.3, 11.4)

Antenna Basics: Introduction, Basic Antenna Parameters, Patterns, Beam Area, Radiation Intensity, Beam Efficiency, Directivity and Gain, Antenna Apertures, Effective Height, Radio Communication Link, Antenna Field Zones. (Text 3: 2.1 - 2.7, 2.9 – 2.11, 2.13)

L1,L2,L3

Module 4

Point Sources and Arrays: Introduction, Point Sources, Power Patterns, Power Theorem, Radiation Intensity, Arrays of two isotropic point sources, Linear Arrays of n Isotropic Point Sources of equal Amplitude and Spacing.
(Text 3: 5.1 – 5.6, 5.9, 5.13)

Electric Dipoles: Introduction, Short Electric Dipole, Fields of a Short Dipole, Radiation Resistance of a Short Electric Dipole, Thin Linear Antenna (Field Analyses)
(Text 3: 6.1 - 6.5)

L1,L2,L3,L4

Module 5

Loop and Horn Antenna: Introduction, Small loop, The Loop Antenna General Case, The Loop Antenna as a special case, Radiation resistance of loops, Directivity of Circular Loop Antennas with uniform current, Horn antennas Rectangular Horn Antennas.
(Text 3: 7.1, 7.2, 7.4, 7.6, 7.7, 7.8, 7.19, 7.20)

Antenna Types: The Helix geometry, Helix modes, Practical Design considerations for the mono-filar axial mode Helical Antenna, Yagi-Uda array, Parabolic reflector
(Text 3: 8.3, 8.4, 8.5, 8.8, 9.5)

L1,L2,L3

Course outcomes: At the end of the course students will be able to:

1. Describe the use and advantages of microwave transmission
2. Analyze various parameters related to microwave transmission lines and waveguides
3. Identify microwave devices for several applications
4. Analyze various antenna parameters necessary for building a RF system
5. Recommend various antenna configurations according to the applications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. **Microwave Engineering** – Annapurna Das, Sisir K Das, TMH, Publication, 2nd, 2010.
2. **Microwave Devices and circuits**- Samuel Y Liao, Pearson Education
3. **Antennas and Wave Propagation**- John D. Krauss, Ronald J Marhefka, Ahmad S Khan, 4th Edition, McGraw Hill Education, 2013

Reference Books:

1. **Microwave Engineering** - David M Pozar, John Wiley India Pvt. Ltd., 3rd Edn, 2008.
2. **Microwave Engineering** – Sushrut Das, Oxford Higher Education, 2nd Edn, 2015
3. **Antennas and Wave Propagation** – Harish and Sachidananda: Oxford University Press, 2007

OPERATING SYSTEM

Course Code	: 18EC641	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (08 Hrs/module)	Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand the services provided by an operating system.
- Explain how processes are synchronized and scheduled.
- Understand different approaches of memory management and virtual memory management.
- Describe the structure and organization of the file system
- Understand interprocess communication and deadlock situations.

Module-1

Introduction to Operating Systems

OS, Goals of an OS, Operation of an OS, Computational Structures, Resource allocation techniques, Efficiency, System Performance and User Convenience, Classes operating System, Batch processing, Multi programming, Time Sharing Systems, Real Time and distributed Operating Systems

(Topics from Sections 1.2, 1.3, 2.2 to 2.8 of Text).

L1,L2

Module-2

Process Management: OS View of Processes, PCB, Fundamental State Transitions of a process, Threads, Kernel and User level Threads, Non-preemptive scheduling- FCFS and SRN, Preemptive Scheduling- RR and LCN, Scheduling in Unix and Scheduling in Linux

(Topics from Sections 3.3, 3.3.1 to 3.3.4, 3.4, 3.4.1, 3.4.2 , Selected scheduling topics from 4.2 and 4.3 , 4.6, 4.7 of Text).

L1,L2,L3

Module – 3

Memory Management: Contiguous Memory allocation, Non-Contiguous Memory Allocation, Paging, Segmentation, Segmentation with paging, Virtual Memory Management, Demand Paging, VM handler, FIFO, LRU page replacement policies, Virtual memory in Unix and Linux

(Topics from Sections 5.5 to 5.9, 6.1 to 6.3 except Optimal policy and 6.3.1, 6.7,6.8 of Text).

L1,L2,L3

Module-4

File Systems: File systems and IOCS, File Operations, File Organizations, Directory structures, File Protection, Interface between File system and IOCS, Allocation of disk space, Implementing file access

(Topics from Sections 7.1 to 7.8 of Text).

L1,L2

Module-5

Message Passing and Deadlocks: Overview of Message Passing, Implementing message passing, Mailboxes, Deadlocks, Deadlocks in resource allocation, Handling deadlocks, Deadlock detection algorithm, Deadlock Prevention

(Topics from Sections 10.1 to 10.3, 11.1 to 11.5 of Text).

L1,L2

Course Outcomes: At the end of the course, the students will be able to:

1. Explain the goals, structure, operation and types of operating systems.
2. Apply scheduling techniques to find performance factors.
3. Explain organization of file systems and IOCS.
4. Apply suitable techniques for contiguous and non-contiguous memory allocation.
5. Describe message passing, deadlock detection and prevention methods.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Operating Systems – A Concept based Approach, by Dhamdhere, TMH, 2nd edition.

Reference Books:

1. Operating Systems Concepts, Silberschatz and Galvin, John Wiley India Pvt. Ltd, 5th edition, 2001.
2. Operating System–Internals and Design System, William Stallings, Pearson Education, 4th ed, 2006.
3. Operating Systems - Design and Implementation, Tanenbaum, TMH, 2001.

ARTIFICIAL NEURAL NETWORKS

Course Code	:18EC642	CIE Marks	: 40
Lecture Hours/Week	:03	SEE Marks	: 60
Total Number of Lecture Hours	: 40(08 Hrs/module)	Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand the basics of ANN and comparison with Human brain.
- Acquire knowledge on Generalization and function approximation of various ANN architectures.
- Understand reinforcement learning using neural networks
- Acquire knowledge of unsupervised learning using neural networks.

Module-1

Introduction: Biological Neuron – Artificial Neural Model - Types of activation functions – **Architecture:** Feedforward and Feedback, Convex Sets, Convex Hull and Linear Separability, Non-Linear Separable Problem. XOR Problem, Multilayer Networks.

Learning: Learning Algorithms, Error correction and Gradient Descent Rules, Learning objective of TLNs, Perceptron Learning Algorithm, Perceptron Convergence Theorem.

L1, L2

Module-2

Supervised Learning: Perceptron learning and Non Separable sets, α -Least Mean Square Learning, MSE Error surface, Steepest Descent Search, μ -LMS approximate to gradient descent, Application of LMS to Noise Cancelling, Multi-layered Network Architecture, Back propagation Learning Algorithm, Practical consideration of BP algorithm.

L1,L2,L3

Module-3

Support Vector Machines and Radial Basis Function: Learning from Examples, Statistical Learning Theory, Support Vector Machines, SVM application to Image Classification, Radial Basis Function Regularization theory, Generalized RBF Networks, Learning in RBFNs, RBF application to face recognition.

L1,L2, L3

Module-4

Attractor Neural Networks: Associative Learning Attractor Associative Memory, Linear Associative memory, Hopfield Network, application of Hopfield Network, Brain State in a Box neural Network, Simulated Annealing, Boltzmann Machine, Bidirectional Associative Memory.

L1,L2, L3

Module-5

Self-organization Feature Map: Maximal Eigenvector Filtering, Extracting Principal Components, Generalized Learning Laws, Vector Quantization, Self-organization Feature Maps, Application of SOM, Growing Neural Gas.

L1,L2, L3

Course Outcomes: At the end of the course, students will be able to:

1. Understand the role of neural networks in engineering, artificial intelligence, and cognitive modelling.
2. Understand the concepts and techniques of neural networks through the study of important neural network models.
3. Evaluate whether neural networks are appropriate to a particular application.
4. Apply neural networks to particular application.
5. Analyze the steps needed to improve performance of the selected neural network.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. **Neural Networks A Classroom Approach**– Satish Kumar, McGraw Hill Education (India) Pvt. Ltd, Second Edition.

Reference Books:

1. **Introduction to Artificial Neural Systems**-J.M. Zurada, Jaico Publications 1994.
2. **Artificial Neural Networks**-B. Yegnanarayana, PHI, New Delhi 1998.

DATA STRUCTURES USING C++

Course Code	: 18EC643	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (08 Hrs/module)	Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to

- Solve the problems using object oriented approach
- Explain fundamentals of data structures and their applications essential for programming/problem solving
- Analyze Linear Data Structures: Stack, Queues, Lists
- Analyze Non Linear Data Structures: Trees
- Assess appropriate data structure during program development/Problem Solving

Module -1

INTRODUCTION: C++ and its features, Data types, Variables, Operators, Expressions, Control structures, classes and Objects, Functions and parameters, function overloading, Recursion, Constructors, Destructors and Operator overloading, Inheritance, Polymorphism, Programming examples.

L1, L2

Module -2

ARRAYS AND MATRICES: Arrays, Matrices, Special matrices, Sparse matrices.

POINTERS: Pointers, Dynamic memory allocation

LINEAR LISTS: Data objects and structures, Introduction to Linear and Non Linear data structures, Linear list data structures, Array Representation, Vector Representation, Singly Linked lists and chains.

L1, L2

Module -3

STACKS: The abstract data types, Array Representation, Linked Representation, Applications – Parsing and Evaluation of arithmetic expressions, Parenthesis Matching & Towers of Hanoi.

L1, L2, L3

Module -4

QUEUES: The abstract data types, Array Representation, Linked Representation, Applications-Railroad car arrangement, Priority Queues

HASHING: Dictionaries, Linear representation, Hash table representation.

L1, L2, L3

Module -5

TREES: Binary trees, Properties and representation of binary trees, Common binary tree operations, Binary tree traversal the ADT binary tree, ADT binary tree and the class linked binary tree. Binary search trees operations and implementation. Heaps, Applications-Heap Sorting

L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

1. Relate to Dynamic memory allocation, Various types of data structures, operations and algorithms and Sparse matrices and Hashing
2. Apply object-oriented approach to solve problems
3. Understand non-Linear data structures trees and their applications
4. Design appropriate data structures for solving computing problems
5. Analyze the operations of Linear Data structures: Stack, Queue and Linked List and their applications

Text Book:

1. Data structures, Algorithms, and applications in C++, Sartaj Sahni, Universities Press, 2nd Edition, 2005.

Reference Books:

2. Object Oriented Programming with C++, E.Balaguruswamy, TMH, 6th Edition, 2013.

DIGITAL SYSTEM DESIGN USING VERILOG

Course Code	:18EC644	CIE Marks	:40
Lecture Hours/Week	:03	SEE Marks	:60
Total Number of Lecture Hours	:40 (08 Hrs/module)	Exam Hours	:03
CREDITS – 03			

Course Learning Objectives: This course will enable students to

- Understand the concepts of Verilog Language.
- Design the digital systems as an activity in a larger systems design context.
- Study the design and operation of semiconductor memories frequently used in application specific digital system.
- Inspect how effectively ICs are embedded in package and assembled in PCBs for different application.
- Design and diagnosis of processors and I/O controllers used in embedded systems.

Module -1

Introduction and Methodology:

Digital Systems and Embedded Systems, Real-World Circuits, Models, Design Methodology **(1.1, 1.3 to 1.5 of Text)**.

Combinational Basics: Combinational Components and Circuits, Verification of Combinational Circuits **(2.3 and 2.4 of Text)**.

Number Basics: Unsigned integers, Signed Integers, Fixed point Numbers, Floating point Numbers **(3.1.1, 3.2.1, 3.3.1 and 3.4)**.

Sequential Basics: Sequential Datapaths and Control Clocked Synchronous Timing Methodology

(4.3 up to 4.3.1, 4.4 up to 4.4.1 of Text).

L1,L2, L3

Module -2

Memories: Concepts, Memory Types, Error Detection and Correction

(Chap 5 of Text).

L1,L2, L3

Module -3

Implementation Fabrics: Integrated Circuits, Programmable Logic Devices, Packaging and Circuit boards, Interconnection and Signal integrity

(Chap 6 of Text).

L1,L2, L3

Module -4

I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software

(Chap 8 of Text).

L1,L2, L3

Module -5

Design Methodology: Design flow, Design optimization, Design for test, Nontechnical Issues
(Chap 10 of Text).

L1,L2, L3, L4

Course outcomes: After studying this course, students will be able to:

1. Construct the combinational circuits, using discrete gates and programmable logic devices.
2. Describe how arithmetic operations can be performed for each kind of code, and also combinational circuits that implement arithmetic operations.
3. Design a semiconductor memory for specific chip design.
4. Design embedded systems using small microcontrollers, larger CPUs/DSPs, or hard or soft processor cores.
5. Synthesize different types of I/O controllers that are used in embedded system.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60

Text Book:

- Peter J. Ashenden, “Digital Design: An Embedded Systems Approach Using VERILOG”, Elsevier, 2010.

Reference Books:

1. Ming-Bo Lin, “Digital System Designs and Practices: Using Verilog HDL and FPGAs”, Wiley, 2008
2. Charles Roth, Lizy K. John, Byeong Kil Lee, “Digital Systems Design Using Verilog”, Cengage, 1st Edition.
3. Donald E. Thomas, Philip R. Moorby, “The Verilog Hardware Description Language”, Springer, Fifth edition.
4. Michael D. Ciletti, “Advanced Digital Design with the Verilog HDL” Pearson (Prentice Hall), Second edition.

NANOELECTRONICS

Course Code	:18EC645	CIE Marks	:40
Lecture Hours/Week	:03	SEE Marks	:60
Total Number of Lecture Hours	:40 (08 Hrs/module)	Exam Hours	:03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Enhance basic engineering science and technical knowledge of Nanoelectronics.
- Explain basics of top-down and bottom-up fabrication process, devices and systems.
- Describe technologies involved in modern day electronic devices.
- Know various nanostructures of carbon and the nature of the carbon bond itself.
- Learn the photo physical properties of sensor used in generating a signal.

Module-1

Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moore's law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometerlength scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems
(Text 1). L1, L2

Module-2

Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques (Text 1).
Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states
(Text 1). L1, L2

Module-3

Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth

of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, colloidal quantum dots, self-assembly techniques. **(Text 1).**

Physical processes: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural

(Text 1).

L1, L2

Module-4

Carbon Nanostructures: Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes.

(Text 2)

L1, L2

Module-5

Nanosensors: Introduction, What is Sensor and Nanosensors?, What makes them Possible?, Order From Chaos, Characterization, Perception, NanosensorsBased On Quantum Size Effects, Electrochemical Sensors, Sensors Based On Physical Properties, Nanobiosensors, Smart dust Sensor for the future. **(Text 3)**

Applications: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS

(Text 1).

L1, L2

Course Outcomes: After studying this course, students will be able to:

1. Construct the combinational circuits, using discrete gates and programmable logic devices.
2. Describe how arithmetic operations can be performed for each kind of code, and also combinational circuits that implement arithmetic operations.
3. Design a semiconductor memory for specific chip design.
4. Design embedded systems using small microcontrollers, larger CPUs/DSPs, or hard or soft processor cores.
5. Synthesize different types of I/O controllers that are used in embedded system.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Edited by Robert Kelsall, Ian Hamley and Mark Geoghegan, "Nanoscale Science and Technology", John Wiley, 2007.
2. Charles P Poole, Jr, Frank J Owens, "Introduction to Nanotechnology", John Wiley, Copyright 2006, Reprint 2011.
3. T Pradeep, "Nano: The essentials-Understanding Nanoscience and Nanotechnology", TMH.

Reference Book:

1. Edited by William A Goddard III, Donald W Brenner, Sergey E. Lyshevski and Gerald J Iafrate, "Hand Book of Nanoscience Engineering and Technology", CRC press, 2003.

PYTHON APPLICATION PROGRAMMING

Course Code	:18EC646	CIE Marks	:40
Lecture Hours/Week	:03	SEE Marks	:60
Total Number of Lecture Hours	:40(08 Hrs/module)	Exam Hours	:03
CREDITS – 03			

Course Learning Objectives: This course will enable students to

- Learn Syntax and Semantics and create Functions in Python.
- Handle Strings and Files in Python.
- Understand Lists, Dictionaries and Regular expressions in Python.
- Implement Object Oriented Programming concepts in Python
- Build Web Services, Network and Database Programs in Python.

Module – 1

Why should you learn to write programs, Variables, expressions and statements, Conditional execution, Functions,

L1, L2, L3

Module – 2

Iteration, Strings, Files,

L1, L2, L3

Module – 3

Lists, Dictionaries, Tuples, Regular Expressions,

L1, L2, L3

Module – 4

Classes and objects, Classes and functions, Classes and methods,

L1, L2, L3

Module – 5

Networked programs, Using Web Services, Using databases and SQL,

L1, L2, L3

Course outcomes: The students will be able to:

1. Examine Python syntax and semantics and be fluent in the use of Python flow control and functions.
2. Demonstrate proficiency in handling Strings and File Systems.
3. Create, run and manipulate Python Programs using core data structures like Lists, Dictionaries and use Regular Expressions.
4. Interpret the concepts of Object-Oriented Programming as used in Python.
5. Implement exemplary applications related to Network Programming, Web Services and Databases in Python.

Question paper pattern:

- The question paper will have TEN questions.
- There will be TWO questions from each module.
- Each question will have questions covering all the topics under a module.
- The students will have to answer FIVE full questions, selecting ONE full question from each module.

Text Books:

1. Charles R. Severance, “Python for Everybody: Exploring Data Using Python 3”, 1st Edition, Create Space Independent Publishing Platform, 2016 (Chapters 1 – 13, 15).
2. Allen B. Downey, “Think Python: How to Think Like a Computer Scientist”, 2nd Edition, Green Tea Press, 2015 (Chapters 15,16,17)

References:

1. Mark Lutz, “Programming Python”, 4th Edition, O’Reilly Media, 2011. ISBN-13:978-9350232873.
2. Wesley J Chun, “Core Python Applications Programming”, 3rd Edition, Pearson Education India, 2015. ISBN-13: 978-9332555365.
3. Reema Thareja, “Python Programming using problem solving approach”, Oxford university press, 2017

SIGNAL PROCESSING

Course Code	: 18EC651	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE Marks	: 60
Total Number of Lecture Hours	: 40 (08 Hrs/module)	Exam Hours	: 03
CREDITS – 03			

Course objective: This course will enable students to:

- Understand, represent and classify continuous time and discrete time signals and systems, together with the representation of LTI systems.
- Ability to represent continuous time signals (both periodic and non-periodic) in the time domain, s-domain and the frequency domain
- Understand the properties of analog filters, and have the ability to design Butterworth filters
- Understand and apply sampling theorem and convert a signal from continuous time to discrete time or from discrete time to continuous time (without loss of information)
- Able to represent the discrete time signal in the frequency domain
- Able to design FIR and IIR filters to meet given specifications

Module-1

Signal Definition, Signal Classification, System definition, System classification, for both continuous time and discrete time. Definition of LTI systems

(Chapter 1)

L1, L2

Module-2

Introduction to Fourier Transform, Fourier Series, Relating the Laplace Transform to Fourier Transform, Frequency response of continuous time systems,

(Chapter 3)

L1, L2

Module-3

Frequency response of ideal analog filters, Salient features of Butterworth filters Design and implementation of Analog Butterworth filters to meet given specifications

(Chapter 8)

L1,L2, L3

Module-4

Sampling Theorem- Statement and proof, converting the analog signal to a digital signal. Practical sampling. The Discrete Fourier Transform, Properties of DFT. Comparing the frequency response of analog and digital systems. (FFT not included)

(Chapter 3, 4)

L1,L2, L3

Module-5

Definition of FIR and IIR filters. Frequency response of ideal digital filters Transforming the Analog Butterworth filter to the Digital IIR Filter using suitable mapping techniques, to meet given specifications. Design of FIR Filters using the Window technique, and the frequency sampling technique to meet given specifications Comparing the designed filter with the desired filter frequency response

(Chapter 8)

L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Understand and explain continuous time and discrete time signals and systems, in time and frequency domain
2. Apply the concepts of signals and systems to obtain the desired parameter/representation
3. Analyse the given system and classify the system/arrive at a suitable conclusion
4. Design analog/digital filters to meet given specifications
5. Design and implement (*assignment component*)
 - a. the analog filter using components/ suitable simulation tools
 - b.the digital filter (FIR/IIR) using suitable simulation tools, and
 - c.record the input and output of the filter for the given audio signal

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- ‘Signals and Systems’, by Simon Haykin and Barry Van Veen, Wiley.

References:

1. ‘Theory and Application of Digital Signal Processing’, Rabiner and Gold
2. ‘Signals and Systems’, Schaum’s Outline series
3. ‘Digital Signal Processing’, Schaum’s Outline series

SENSORS and SIGNAL CONDITIONING

Course Code	: 18EC652	CIE Marks	: 40
Lecture Hours/Week	: 03	SEE marks	: 60
Total Number of Lecture Hours	: 40 (08 Hrs/module)	Exam Hours	: 03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand various technologies associated in manufacturing of sensors
- Acquire knowledge about types of sensors used in modern digital systems
- Get acquainted about material properties required to make sensors

Module 1

Introduction to sensor based measurement systems:

General concepts and terminology, sensor classification, primary sensors, material for sensors, microsensor technology, magnetoresistors, light dependent resistors, resistive hygrometers, resistive gas sensors, liquid conductivity sensors

(Selected topics from ch.1 & 2 of Text)

L1, L2

Module 2

Reactance Variation and Electromagnetic Sensors: -Capacitive Sensors, Inductive Sensors, Electromagnetic Sensors.

Signal Conditioning for Reactance Variation Sensors-Problems and Alternatives, ac Bridges Carrier Amplifiers, Coherent Detection, Specific Signal Conditioners for Capacitive Sensors, Resolver-to-Digital and Digital-to-Resolver Converters.

L1, L2

Module 3

Self-generating Sensors-Thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors.

L2, L3

Module 4

Digital and intelligent sensors-position encoders, resonant sensors, sensors based on quartz resonators, SAW sensors, Vibrating wire strain gages, vibrating cylinder sensors, Digital flow meters.

L2, L3

Module 5

Sensors based on semiconductor junctions -Thermometers based on semiconductor junctions, magneto diodes and magneto transistors, photodiodes and phototransistors, sensors based on MOSFET transistors, charge- coupled sensors – types of CCD imaging sensors, ultrasonic-based sensors.

L2, L3

Course Outcomes: After studying this course, students will be able to:

1. Appreciate various types of sensors
2. Describe the manufacturing process of sensors
3. Understand about the material properties required to make sensors
4. Use sensors specific to the end use application
5. Design systems integrated with sensors

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

“Sensors and Signal Conditioning”, Ramon PallásAreny, John G. Webster, 2nd edition, John Wiley and Sons, 2000

ADDITIONAL OPEN ELECTIVES-A OFFERED BY EC/TC BOARD

B. E. EC/TE Choice Based Credit System (CBCS) and Outcome Based Education (OBE) SEMESTER – VI			
VIRTUAL INSTRUMENTATION			
Course Code	18EC653	CIE Marks	40
Number of Lecture Hours/Week	03	SEE Marks	60
Total Number of Lecture Hours	40(8Hours/Module)	Exam Hours	03
CREDITS – 03			
Course objective: This course will enable students to: <ul style="list-style-type: none"> • Understand the fundamental principles of virtual instrumentation • Acquire, analyze and present data using LabVIEW 			
Module-1			RBT Level
Graphical System Design: Introduction, Graphical system design model, Design flow with GSD, Virtual Instrumentation, Virtual instrument and traditional instrument, Hardware and software in virtual instrumentation, Virtual instrumentation for Test, control & design, Graphical system design using LABVIEW, Graphical programming & textual programming.			L1, L2, L3
Module-2			
Introduction to LabVIEW: Introduction, advantages of LABVIEW software environment, palettes, front panel controls & indicators, Block diagram, Data flow program. Repetition and Loops: For loops, while loops, structure tunnels, terminals inside or outside loops, shift registers, feed-back nodes, control timing, case structure.			L1, L2, L3
Module-3			
Arrays: Introduction, arrays in LABVIEW, creating one - dimensional array controls, indicators and constants, creating two dimensional arrays, creating multidimensional arrays, initializing array, deleting, inserting, and replacing elements, rows, columns, and pages with in arrays, arrays functions.			L1, L2, L3
Module-4			
Plotting Data: Types of waveforms, waveform graphs, waveform charts, XY graphs, Intensity graphs & charts, Digital waveform graphs, 3D graphs, customizing graphs & charts, configuring a graph or chart, Displaying special planners on the XY graph.			L1,L2, L3
Module-5			
File Input/ Output: File formats, file write &read, generating filenames automatically, String handling: string functions, LABVIEW string formats, parsing of strings. Instrument Control: Introduction, GPIB communication, Hardware specification, software architecture, Instrument I/O assistant, VISA, Instrument drivers, serial port communications, using other interfaces.			L1, L2, L3
Course Outcomes: After studying this course, students will be able to: <ol style="list-style-type: none"> 1. Recognize the Graphical system design model and develop programs using the modern tools of Graphical programming & textual programming 2. Develop a virtual instrumentation model using the front panel controls & indicators and loops. 3. Analyze, design the various array and matrix operations using LabVIEW functions. 4. Evaluate the various forms of output representations using graphs & charts 5. Demonstrate Instrument Control, GPIB communication and other interfaces 			

Students have to conduct the following experiments as a part of CIE marks along with other Activities:

1. Build a VI code to indicate the change in temperature using LabVIEW
2. Develop a code in VI to convert 4-bit binary input to gray output using LabVIEW
3. Generate a VI code to display sinusoidal and triangular waveforms using LabVIEW
4. Build a code using LabVIEW to compute the sum of N numbers (use FOR loop)
5. Develop a VI code using LabVIEW to sort the even numbers (use while loop)
6. Using LabVIEW compute the basic operations of a simple calculator using case structure

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. "Virtual Instrumentation using LABVIEW", Jovitha Jerome, PHI, 2010
2. "Virtual Instrumentation using LABVIEW", Sanjay Gupta, Joseph John, TMH, McGraw Hill Second Edition, 2011.

Reference:

"Learning with LabView", Robert H Bishop, Prentice Hall, 2009.

ADDITIONAL OPEN ELECTIVES-A OFFERED BY EC/TC BOARD

B. E. EC/TE			
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)			
SEMESTER – VI			
MICROCONTROLLERS			
Course Code	18EC654	CIE Marks	40
Number of Lecture Hours/Week	03	SEE Marks	60
Total Number of Lecture Hours	40(8Hours/Module)	Exam Hours	03
CREDITS – 03			
<p>Course objective: This course will enable students to:</p> <ul style="list-style-type: none"> • Learn architecture of 8051. • Learn programming skills using Assembly language and C • Design and interface microcontroller based embedded systems. • Build projects 			
Module-1			RBT Level
<p>Microprocessors and Microcontroller: Introduction, Microprocessors and Microcontrollers, Microcontroller Survey. (Text 1- Chapter 1) The 8051 Architecture: Introduction, Architecture of 8051, Pin diagram of 8051, Memory organization. (Text 1- Chapter 2)</p>			L1, L2
Module-2			
<p>Addressing Modes in 8051 Microcontroller: Introduction, Addressing Modes, External Data Moves, Code Memory Read only Data Moves, PUSH and POP opcodes, Data Exchanges, Example Programs. (Text 1- Chapter 3)</p>			L1, L2
Module-3			
<p>Instruction set: Instruction timings, 8051 instructions: Data transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Subroutine instructions, Bit manipulation instruction. (Text 1- Chapter 4, 5 and 6)</p>			L1, L2, L3
Module-4			
<p>8051 Microcontroller Interfacing and Applications: Interfacing 8051 to LCD, Keyboard, parallel and serial ADC, DAC interfacing and programming. (Text 2 – Chapter 12 and 13)</p>			L1,L2, L3
Module-5			
<p>8051 Microcontroller Interrupts and Timers/counters: Basics of interrupts, 8051 interrupt structure, Timers and Counters, 8051 timers/counters, programming 8051 timers in assembly and C . (Text 2 – Chapter 9, Chapter 11 -11.1) 8051 Microcontroller Serial Communication: Data communication, Basics of Serial Data Communication, 8051 Serial Communication, connections to RS-232, Serial communication Programming in assembly and C. (Text 2 – Chapter 10- 10.1,10.2, 10.3)</p>			L1, L2, L3
<p>Course Outcomes: After studying this course, students will be able to:</p> <ol style="list-style-type: none"> 1. Explain the basics of Microprocessor and Microcontroller 2. Relate to the 8051 Microcontroller architecture and Pin description 3. Analyze 8051 Addressing modes and use the 8051 instruction set 4. Program the on-chip peripherals in 8051 5. Design and develop applications using 8051 Assembly language and C program 			
<p>Students have to conduct the following experiments as a part of CIE marks along with other Activities:</p> <ol style="list-style-type: none"> 1. Write an 8051 ALP to exchange n = 5 bytes of data at location 0027H and at location 0041H. 2. Write an 8051 ALP to sort an array of n = 6 bytes of data in ascending order stored from location 9000H.(use bubble sort algorithm) 			

3. Write an 8051 ALP to implement (display) an eight bit up/down binary (hex) counters on watch window.
4. Write a program to toggle all the bits of P1 and P2 continuously using CALL and RETURN instructions
5. Write an 8051 ALP to implement ASCII to hexadecimal conversion
6. Write a Program illustrating timer delay Generate a 1second delay continuously using the on-chip timer in interrupt mode.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. "The 8051 Microcontroller Architecture, Programming and Applications", Kenneth J Ayala, Thomson learning, 2005.
2. "The 8051 Microcontroller and Embedded Systems-using Assembly and C", Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D McKinaly, Pearson, 2006.

Reference:

"The 8051 Microcontroller: Hardware, Software and Applications" V. Udayashankara and Mallikarjuna Swamy, TMH., 2009.

ADDITIONAL OPEN ELECTIVES-A OFFERED BY EC/TC BOARD

B. E. EC/TE Choice Based Credit System (CBCS) and Outcome Based Education (OBE) SEMESTER – VI			
BASIC VLSI DESIGN			
Course Code	18EC655	CIE Marks	40
Number of Lecture Hours/Week	03	SEE Marks	60
Total Number of Lecture Hours	40(8Hours/Module)	Exam Hours	03
CREDITS – 03			
Course objective: This course will enable students to: <ul style="list-style-type: none"> • Understand the fundamental aspects of circuits in silicon • Relate to VLSI design processes and design rules 			
Module-1			RBT Level
Moore’s law, speed power performance, nMOS fabrication, CMOS fabrication: n-well, p-well processes, BiCMOS, Comparison of bipolar and CMOS. Basic Electrical Properties of MOS And BiCMOS Circuits: Drain to source current versus voltage characteristics, threshold voltage, transconductance.			L1, L2
Module-2			
Basic Electrical Properties of MOS And BiCMOS Circuits: nMOS inverter, Determination of pull up to pull down ratio: nMOS inverter driven through one or more pass transistors, alternative forms of pull up, CMOS inverter, BiCMOS inverters, latch up. Basic Circuit Concepts: Sheet resistance, area capacitance calculation, Delay unit, inverter delay, estimation of CMOS inverter delay, super buffers, BiCMOS drivers.			L1, L2
Module-3			
MOS and BiCMOS Circuit Design Processes: MOS layers, stick diagrams, nMOS design style, CMOS design style Design rules and layout & Scaling of MOS Circuits: λ - based design rules, scaling factors for device parameters			L1, L2, L3
Module-4			
Subsystem Design and Layout-1: Switch logic pass transistor, Gate logic inverter, NAND gates, NOR gates, pseudo nMOS, Dynamic CMOS Examples of structured design: Parity generator, Bus arbitration, multiplexers, logic function block, code converter.			L1,L2, L3
Module-5			
Subsystem Design and Layout-2: Clocked sequential circuits, dynamic shift registers, bus lines, General considerations, 4-bit arithmetic processes, 4-bit shifter, Regularity-Definition & Computation Practical aspects and testability: Some thoughts of performance, optimization and CAD tools for design and simulation.			L1, L2, L3
Course Outcomes: After studying this course, students will be able to: <ol style="list-style-type: none"> 1. Identify the CMOS layout levels, and the design layers used in the process sequence. 2. Describe the general steps required for processing of CMOS integrated circuits. 3. Design static CMOS combinational and sequential logic at the transistor level. 4. Demonstrate different logic styles such as complementary CMOS logic, pass-transistor Logic, dynamic logic, etc. 5. Interpret the need for testability and testing methods in VLSI. 			

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

“Basic VLSI Design”, Douglas A Pucknell, Kamran Eshraghian, 3rd Edition, Prentice Hall of India publication, 2005.

References:

1. “CMOS Digital Integrated Circuits, Analysis And Design”, Sung – Mo (Steve) Kang, Yusuf Leblebici, Tata McGraw Hill, 3rd Edition, 2003.
2. “VLSI Technology”, S.M. Sze, 2nd edition, Tata McGraw Hill, 2003.

EMBEDDED SYSTEMS LABORATORY

Course Code : 18ECL66	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level : L1, L2, L3	Exam Hours : 03	
CREDITS–02		

Course Learning Objectives: This course will enable students to:

- Understand the instruction set of ARM Cortex M3, a 32 bit microcontroller and the software tool required for programming in Assembly and C language.
- Program ARM Cortex M3 using the various instructions in assembly level language for different applications.
- Interface external devices and I/O with ARM Cortex M3.
- Develop C language programs and library functions for embedded system applications.

Laboratory Experiments

Conduct the following experiments on an ARM CORTEX M3 evaluation board to learn ALP and using evaluation version of Embedded 'C' & Keil uVision-4 tool/compiler.

PART A:

1. ALP to multiply two 16 bit binary numbers.
2. ALP to find the sum of first 10 integer numbers.
3. ALP to find the number of 0's and 1's in a 32 bit data
4. ALP to find determine whether the given 16 bit is even or odd
5. ALP to write data to RAM

PART B:

6. Display "Hello world" message using internal UART
7. Interface and Control the speed of a DC Motor.
8. Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction.
9. Interface a DAC and generate Triangular and Square waveforms.
10. Interface a 4x4 keyboard and display the key code on an LCD.
11. Demonstrate the use of an external interrupt to toggle an LED On/Off.
12. Display the Hex digits 0 to F on a 7-segment LED interface, with an appropriate delay.
13. Measure Ambient temperature using a sensor and SPI ADC IC.

Course outcomes: After studying this course, students will be able to:

1. Understand the instruction set of 32 bit microcontroller ARM Cortex M3, and the software tool required for programming in Assembly and C language.
2. Develop assembly language programs using ARM Cortex M3 for different applications.
3. Interface external devices and I/O with ARM Cortex M3.
4. Develop C language programs and library functions for embedded system applications.
5. Analyze the functions of various peripherals, peripheral registers and power saving modes of ARM Cortex M3

Conduction of Practical Examination:

- One Question from PART A and one Question from PART B to be asked in the examination.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

COMMUNICATION LABORATORY

Course Code : 18ECL67	CIE Marks : 40	SEE Marks : 60
Lecture Hours/Week: 02 Hours Tutorial (Instructions) + 02 Hours Laboratory		
RBT Level: L1, L2, L3	Exam Hours : 03	
CREDITS – 02		

Course Learning Objectives: This course will enable students to:

- Design and test the communication circuits for different analog modulation schemes.
- Design and demonstrate the digital modulation techniques
- Demonstrate and measure the wave propagation in microstrip antennas
- Characteristics of microstrip devices and measurement of its parameters.
- Understand the probability of error computations of coherent digital modulation schemes.

Laboratory Experiments

PART-A: Expt. 1 to Expt. 5 have to be performed using discrete components.

1. Amplitude Modulation and Demodulation: i) Standard AM, ii) DSBSC (LM741 and LF398 ICs can be used)
2. Frequency modulation and demodulation (IC 8038/2206 can be used)
3. Pulse sampling, flat top sampling and reconstruction
4. Time Division Multiplexing and Demultiplexing of two bandlimited signals.
5. FSK and PSK generation and detection
6. Measurement of frequency, guide wavelength, power, VSWR and attenuation in microwave test bench.
7. Obtain the Radiation Pattern and Measurement of directivity and gain of microstrip dipole and Yagi antennas.
8. Determination of
 - a. Coupling and isolation characteristics of microstrip directional coupler.
 - b. Resonance characteristics of microstrip ring resonator and computation of dielectric constant of the substrate.
 - c. Power division and isolation of microstrip power divider.

PART-B: Simulation Experiments using SCILAB/MATLAB/Simulink or LabVIEW

1. To Simulate NRZ, RZ, half-sinusoid & raised cosine pulses and generate eye diagram for binary polar signaling.
2. Pulse code modulation and demodulation system.

3. Computations of the Probability of bit error for coherent binary ASK, FSK and PSK for an AWGN Channel and compare them with their performance curves.
4. Digital Modulation Schemes i) DPSK Transmitter and Receiver, ii) QPSK Transmitter and Receiver.

Course Outcomes: On the completion of this laboratory course, the students will be able to:

1. Design and test circuits for analog modulation and demodulation schemes viz., AM, FM, etc.
2. Determine the characteristics and response of microwave waveguide.
3. Determine characteristics of microstrip antennas and devices & compute the parameters associated with it.
4. Design and test the digital and analog modulation circuits and display the waveforms.
5. Simulate the digital modulation systems and compare the error performance of basic digital modulation schemes.

Conduct of Practical Examination:

- All laboratory experiments are to be considered for practical examination.
- For examination one question from **PART-A** and one question from **PART-B** or only one question from **PART-B** experiments based on the complexity, to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.