MITE
Invent Solutions

MANGALORE INSTITUTE OF TECHNOLOGY & ENGINEERING
(A Unit of Rajalaxmi Education Trust®, Mangalore)
Autonomous Institute affiliated to VTU, Belagavi, Approved by AICTE, New Delhi
Accredited by NAAC with A+ Grade & ISO 9001:2015 Certified Institution

Model Question Paper

Third Semester BE Degree Examination

Computer Organization

Time: 3 Hours **Max. Marks: 100**

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M: Marks, L: RBT (Revised Bloom's Taxonomy) level, C: Course outcomes.

		Module -1	M	L	C
Q1	a.	Explain the operational concepts of a computer and Illustrate with a neat diagram how processor and memory are interconnected.	08	L2	CO1
	b.	Define addressing mode? Describe any four addressing modes with the help of examples for each.	08	L2	CO1
	c.	Compare RISC and CISC architecture	04	L2	CO1
		OR			
Q2	a.	Illustrate the term byte addressability. Describe Big-Endian and Little-Endian byte address assignments with an example.	08	L2	CO1
	b.	What is an assembler directive? Illustrate the role of ORIGIN and RESERVE assembler directives in assembly language programming with the help of an example code segment.	08	L2	CO1
	c.	Summarize the factors that affect the performance of computers.	04	L2	CO1
		Module- 2			
Q3	a.	Describe various registers used in the keyboard interface. Build a code segment for reading a character from the keyboard.	07	L3	CO2
	b.	Given 32K words of main memory, 1K words of cache memory and block size is 16 words. Identify number of bits required for different fields for direct mapped cache.	07	L3	CO2
	c.	Given a 32X32 memory cell array, identify how much address lines are required to address the memory and also the address lines required for selecting row and column when 1K X 1 memory chip is constructed using above array of memory cells.	06	L3	CO2
		OR			
Q4	a.	Calculate the average access time experienced by the processor, if cache hit rate is 0.88, miss penalty is 0.02 milliseconds and cache access time is 10 micro seconds	07	L3	CO2
	b.	Build a memory of 2M words of 32 bits each (2M X 32) memory using 512KB X 8 static memory chip	07	L3	CO2
	c.	Build a RICS style program that reads a line of character and display it.	06	L3	CO2
		Module - 3			
Q5	a.	Build a n-bit binary addition/subtraction logic circuit	07	L3	CO3
	b.	Identify gate delay in 4 bit ripple carry adder and 4-bit carry-lookahead adder	07	L3	CO3
	c.	Apply Booths algorithm to multiply 14 and -5	06	L3	CO3
		OR			

Q6	a.	Build a 16-bit carry lookahead adder and describe the delay of the circuit to find the sum and carry	07	L3	CO3
	b.	Describe non-restoring division algorithm and apply same to divide 8 by 3	07	L3	CO3
	c.	Show the hardware configuration of a sequential multiplier and multiply 13 and 12 using sequential multiplication.	06	L3	CO3
Module - 4					
Q7	a.	Explain single bus organization of datapath in the processor. Develop control sequence for MOVE (R1), R2	06	L3	CO3
	b.	Develop sequence of actions needed to fetch and execute the instruction And X(R7), R9	06	L3	CO3
	c.	Develop micro routine for complete execution of Add (R3), R1	08	L3	CO3
OR					
Q8	a.	Develop the control sequence for complete execution of Add (R3), R1	06	L3	CO3
	b.	Explain Three bus organization of the data path in the processor. Develop the control sequence for Add R1,R2,R3	06	L3	CO3
	c.	Describe the organization of control unit to allow branching in microprograme. Develop micro routine for Branch < 0.	08	L3	CO3
Module - 5					
Q9	a.	A program contains 20 instructions, each instructions requires 5 cycles to complete the executions. Identify the performance improvement in the complete execution of the program in non pipeline and 5 stage pipelined organization. Consider ideal case for pipeline and each stage is completed in one cycle.	07	L3	CO4
	b.	Consider Add R2, R3,#100 Subtract R9,R2,#30 Identify number of stall in the pipeline and explain the reason for the same.	07	L3	CO4
	c.	Explain a 2-state machine representation of branch prediction algorithms. Consider a program with a loop that executes 1000 times. Every iteration of the loop has a branch at the end, where 75% of the branches are taken, and 25% are not taken. Using a 2-state branch predictor (Predict Taken, Predict Not Taken), how accurate would the predictions be by the end of the loop execution	06	L3	CO4
OR					
Q10	a.	How data dependencies are handled in software. Apply the same to handle data dependency in the following code Add R2, R3,#100 Subtract R9,R2,#30	07	L3	CO4
	b.	Add R2,R3,#100 Load R5, 16(R6) Subtract R7,R8,R9 Store R10,24(R11) Develop the instruction flow for the above instruction in a super scalar processor with two execution units	07	L3	CO4
	c.	Explain 4-state machine representation of branch prediction algorithms. A program contains a loop that executes 20 times. In the first 8 iterations, a branch is consistently taken. For the next 6 iterations, the branch alternates between taken and not taken every other time. In the final 6 iterations, the branch is consistently not taken. Using a 4-state branch predictor Calculate the predictor's accuracy for each phase and the overall accuracy by the end of the 20 iterations.	06	L3	CO4

-*****-