Module 3

Operational Amplifier and 555 Timer

Syllabus:

Operational Amplifier: Block diagram, Ideal Op-amp, Op-amp parameters, Inverting and Non-Inverting Op-amp circuits, Op-amp applications: Voltage follower, Adder, Subtractor, Integrator, Differentiator, Comparator, Schmitt trigger, Wein Bridge Oscillator.
IC 555 Timer and Astable Oscillator using IC 555.

3. INTRODUCTION:

An operational amplifier is a direct-coupled high-gain amplifier usually consisting of one or more differential amplifiers and usually followed by a level translator and an output stage. An operational amplifier is available as a single integrated circuit package. The operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for computing such mathematical functions as addition, subtraction, multiplication, and integration. Thus the name operational amplifier stems from its original use for these mathematical operations and is abbreviated to op-amp. With the addition of suitable external feedback components, the modern day op-amp can be used for a variety of applications, such as ac and dc signal amplification, active filters, oscillators, comparators, regulators, and others.

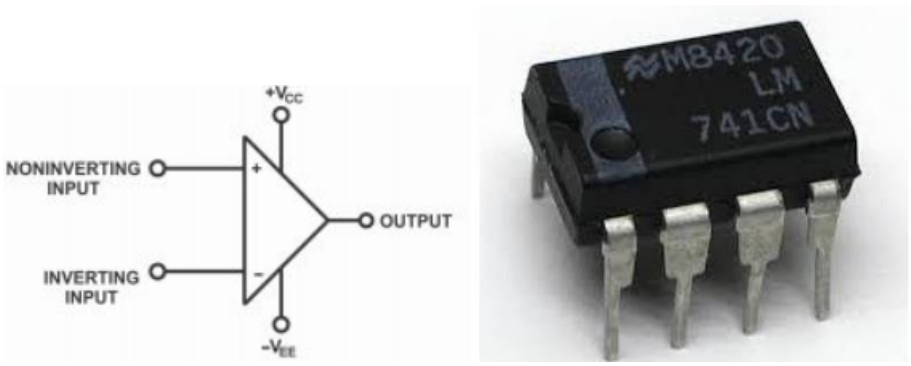

Fig 3.1 Op-Amp circuit symbol

3.1 BLOCK DIAGRAM

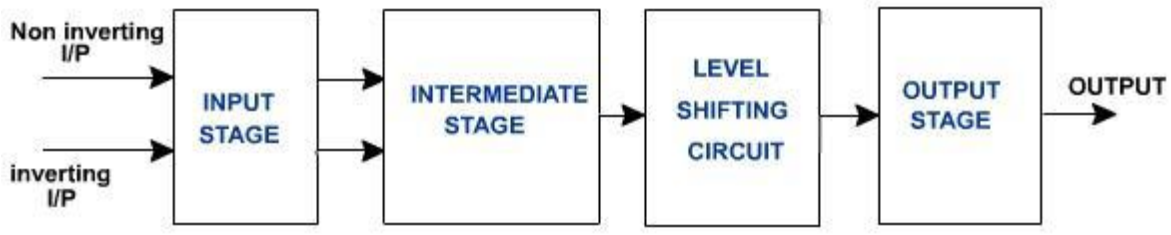

Fig 3.2 Block diagram of Op-Amp

An Operational Amplifier is basically a three-terminal device which consists of two high impedance inputs. One of the inputs is called the Inverting Input, marked with a negative or “minus” sign, (–). The other input is called the Non-inverting Input, marked with a positive or “plus” sign (+). A third terminal represents the operational amplifiers output port which can both sink and source either a voltage or a current. In a linear operational amplifier,

the output signal is the amplification factor, known as the amplifiers gain (A) multiplied by the value of the input signal and depending on the nature of these input and output signals, there can be four different classifications of operational amplifier gain.

1. Input Stage:

- Dual i/p, Balanced o/p Diff. Amplifier
- The i/p stage should have the following characteristics:
- High i/p resistance (typ. 10M ohm)
- Low i/p bias current (typ. 0.5 micro Amp.)
- Small input offset voltage (typ. 10 mV)
- Small input offset current (typ. 0.2 mA)
- High CMRR (typ. 70 dB)
- High Open-loop voltage gain (typ. 104)
- Provides
- Most voltage gain of Op-Amp
- I/p resistance of Op-Amp

2. Intermediate Stage:

- Dual i/p, Unbalanced o/p Diff Amplifier
- Drives the o/p of 1st stage
- Direct coupling, dc voltage well above ground level
- Increases the overall gain of op-amp

3. Level Translator (or) Shifting Stage:

- Dc voltage level is shifted to zero w.r.t ground
- It is the emitter follower with constant current source

4. Output Stage:

- Increases o/p voltage swing
- Raises current supply capability of Op-Amp
- Low Resistance
- Complementary symmetry push-pull amplifier
- It should have following characteristics:
- Large output voltage swing capability

- Large output voltage swing capability

- Low output resistance
- Short circuit protection

3.2 IDEAL OPERATIONAL AMPLIFIER:

This op-amp is said to be ideal if it has the following characteristics.

Open loop voltage gain, $A_{OL} = \infty$
Input impedance, $R_i = \infty$
Output impedance, $R_o = 0$
Bandwidth $BW = \infty$
Zero offset, i.e. $v_o = 0$ **when** $v_1 = v_2 = 0$**.**

(i) an ideal op-amp draws no current at both the input terminals i.e., $i_1 = i_2 = 0$. Because of infinite input impedance, any signal source can drive it and there is no loading on the preceding driver stage.

(ii) Since gain is ∞, the voltage between the inverting and non-inverting terminals, i.e., differential input voltage $v_d = (v_1 - v_2)$ is essentially zero for finite output voltage v_o.

(iii) The output voltage v_o is independent of the current drawn from the output as $R_o = 0$. The output thus can drive an infinite number of other devices.

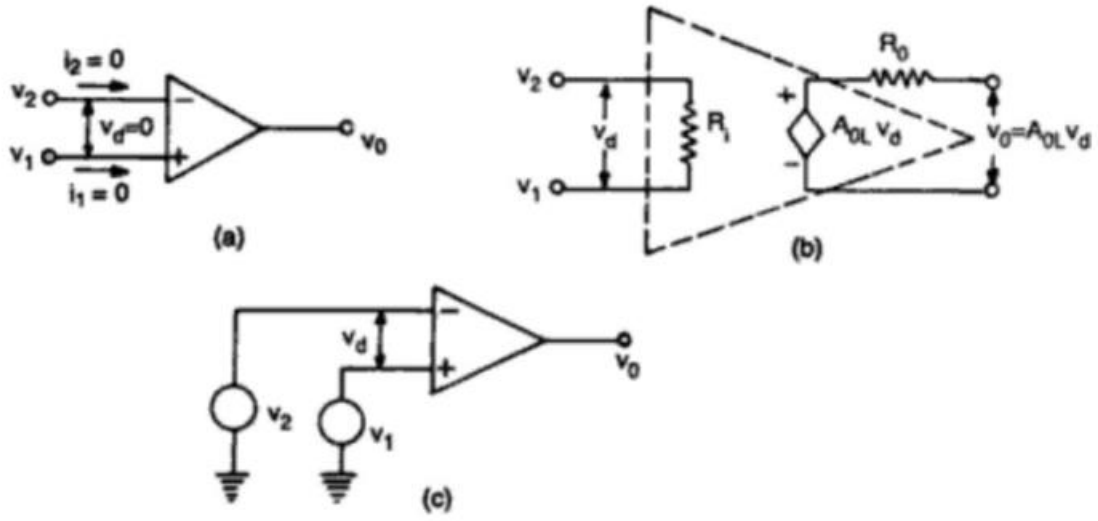

Fig 3.3 (a) Ideal op-amp (b) Equivalent circuit of an op-amp (c) Open loop circuit

IDEAL VOLTAGE TRANSFER CURVE:

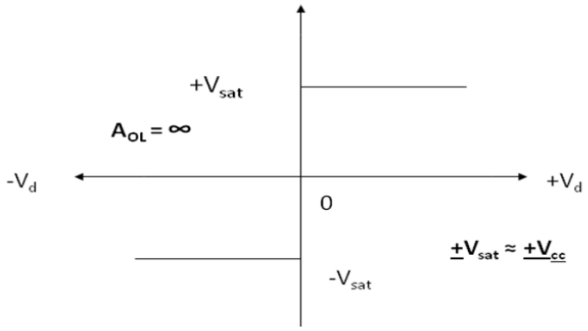

Fig 3.4 V-I characteristic of ideal op-amp

PRACTICAL OP-AMPLIFIER:

- The open loop gain of practical Op – Amp is around 7000.
- Practical Op – Amp has non zero offset voltage. That is, the zero output is obtained for the non – zero differential input voltage only.
- The bandwidth of practical Op – Amp is very small value. This can be increased to desired value by applying an adequate negative feedback to the Op – Amp.
- The output impedance is in the order of hundreds. This can be minimized by applying an adequate negative feedback to the Op – Amp.
- The input impedance is in the order of Mega Ohms only. (Whereas the ideal Op – Amp has infinite input impedance).

DIFFERENCES BETWEEN IDEAL AND PRACTICAL OP-AMPS:

Characteristics	Ideal Op-amp	PracticalOp-amp
Voltage gain	Infinite	High
Input resistance	Infinite	High
Output resistance	Zero	Low
Outputvoltagewheninputvoltageis zero	Zero	Low
Band width	Infinite	High
CMRR	Infinite	High
Slew Rate	Infinite	High

3.3 OP-AMP PARAMETERS:

- **Open Loop Gain, (Avo)**
- Infinite – The main function of an operational amplifier is to amplify the input signal and the more open loop gain it has the better. Open-loop gain is the gain of the op-amp without positive or negative feedback and for such an amplifier the gain will be infinite but typical real values range from about 20,000 to 200,000.
- **Input impedance, (ZIN)**
- Infinite – Input impedance is the ratio of input voltage to input current and is assumed to be infinite to prevent any current flowing from the source supply into the amplifiers input circuitry (IIN = 0). Real op-amps have input leakage currents from a few pico-amps to a few milli-amps.

- **Output impedance, (ZOUT)**
- Zero – The output impedance of the ideal operational amplifier is assumed to be zero acting as a perfect internal voltage source with no internal resistance so that it can supply as much current as necessary to the load. This internal resistance is effectively in series with the load thereby reducing the output voltage available to the load. Real op-amps have output impedances in the 100-20kΩ range.

- **Bandwidth, (BW)**
- Infinite – An ideal operational amplifier has an infinite frequency response and can amplify any frequency signal from DC to the highest AC frequencies so it is therefore assumed to have an infinite bandwidth. With real op-amps,the bandwidth is limited by the Gain-Bandwidth product (GB), which is equal to the frequency where the amplifiers gain becomes unity.

- **Offset Voltage, (VIO)**
- Zero – The amplifiers output will be zero when the voltage difference
- between the inverting and the non-inverting inputs is zero, the same or when both inputs are grounded. Real op-amps have some amount of

output offset voltage.From these "idealized" characteristics above, we can see that the input resistance is infinite, so no current flows into either input terminal (the "current rule") and that the differential input offset voltage is zero (the "voltage rule").

- It is important to remember these two properties as they will help us understand the workings of the Operational Amplifier with regards to the analysis and design of op-amp circuits.
- However, real Operational Amplifiers such as the commonly available uA741, for example do not have infinite gain or bandwidth but have a typical "Open Loop Gain" which is defined as the amplifiers output amplification without any external feedback signals connected to it and for a typical operational amplifier is about 100dB at DC (zero Hz).

$$\text{Voltage Gain, (A)} = \frac{V_{out}}{V_{in}}$$

$$20\log(A) \text{ or } 20\log\frac{V_{out}}{V_{in}} \textit{ in dB}$$

- **Output offset Voltage**

  With 0 volts applied to the inputs of an op amp, we expect to find 0 volts at the output. In fact, we will find a small DC offset present at the output. This is called the output offset voltage and is a result of the combined effects of bias current

- **Input offset current**

  The input offset current (I_{OS}) is equal to the difference between the input bias current at the non-inverting terminal (I_{B+}) minus the input bias current at the inverting (I_{B-}) terminal of the amplifier.

- **Input bias current**

  The input bias current parameter, I_{IB}, is defined as the average of the currents into the two input terminals with the output at a specified level. It is expressed in units of amperes.

3.4 .1 INVERTING AMPLIFIER:

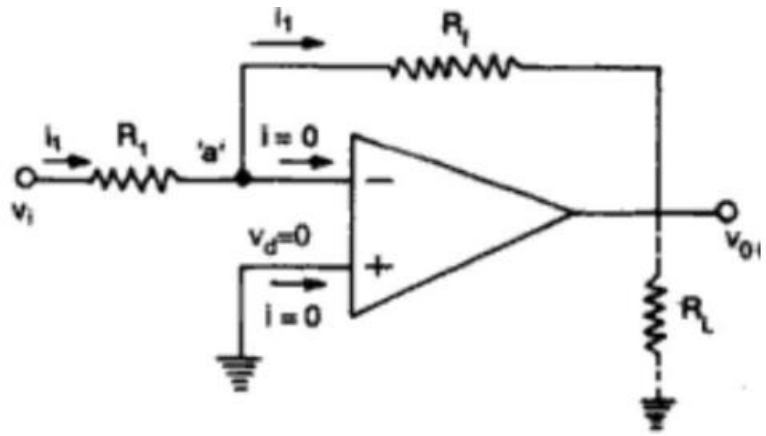

Fig 3.5 (a) Inverting amplifier

Analysis:

For simplicity, assume an ideal op-amp. As v_d=0, node 'a' is at ground potential and the current $i_1$through R_1 is

$$i_1 = \frac{v_i}{R_1}$$

Also, since op-amp draws no current, all the current flowing through R_1 must flow through R_f The output voltage,

$$v_0 = -i_1 R_f = -v_i \frac{R_f}{R_1}$$

Hence, the gain of the inverting amplifier (also referred as closed loop gain) is,

$$A_{CL} = \frac{v_0}{v_i} = -\frac{R_f}{R_1}$$

Alternatively, the nodal equation at the node 'a' in Fig. 3.5 (a) is

$$\frac{v_a - v_i}{R_1} + \frac{v_a - v_o}{R_f} = 0$$

where v_a is the voltage at node 'a'. Since node 'a' is at virtual ground, v_a=0. Therefore we get,

$$A_{CL} = \frac{v_0}{v_i} = -\frac{R_f}{R_1}$$

The negative sign indicates a phase shift of 180 degrees between v_i and v_o.

Example 1

Design an amplifier with a gain of **-10** and input resistance equal to **10 kΩ**.

Solution

Since the gain of the amplifier is negative, an **inverting amplifier** has to be made.

In Fig. 2.5 (a) choose $R_1 = 10\ \text{k}\Omega$

Then $R_f = -A_{CL}R_1$ (from Eq. 2.4)
$= -(-10) \times 10\ \text{k}\Omega = 100\ \text{k}\Omega$

Example 2

In Fig. 2.5 (b), $R_1 = 10\ \text{k}\Omega, R_f = 100\ \text{k}\Omega, v_i = 1\ \text{V}$. A load of $25\ \text{k}\Omega$ is connected to the output terminal. Calculate (i) i_1, (ii) v_o, (iii) i_L and total current i_o into the output pin.

Solution

(a) $i_1 = \frac{v_i}{R_1} = \frac{1\ \text{V}}{10\ \text{k}\Omega} = 0.1\ \text{mA}$

(b) $v_o = -\frac{R_f}{R_1}v_i = -\frac{100\ \text{k}\Omega}{10\ \text{k}\Omega}(1\ \text{V}) = -10\ \text{V}$

(c) $i_L = \frac{v_o}{R_L} = \frac{-10\ \text{V}}{25\ \text{k}\Omega} = -0.4\ \text{mA}.$
The direction of i_L is shown in Fig. 2.5 (b).

(d) i_1 as calculated above is $0.1\ \text{mA}$.

Therefore, total current $i_o = i_1 + i_L = 0.1\ \text{mA} + 0.4\ \text{mA} = 0.5\ \text{mA}$.

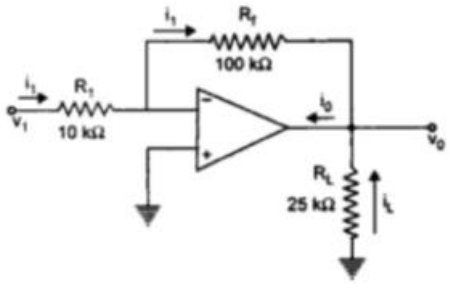

Fig 3.6 Circuit for example 2.2

3.4.2 NON-INVERTING AMPLIFIER:

If the signal is applied to the non-inverting input terminal and feedback is given as shown in fig, the circuit amplifies without inverting the input signal. Such a circuit is called non-inverting amplifier. Negative feedback system as output is being fed back to the inverting input terminal.

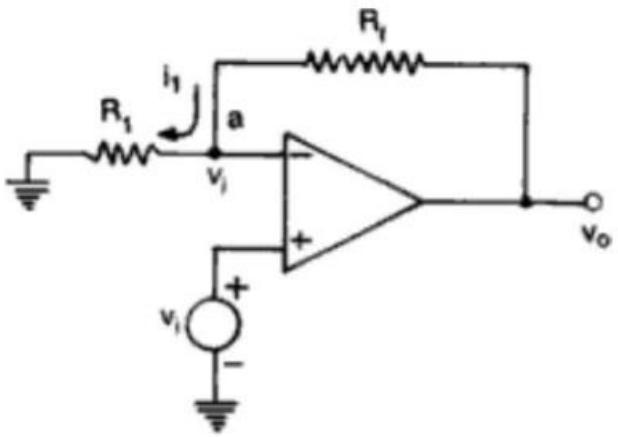

Fig 3.7 Non-inverting amplifier

As the differential voltage v_d at the input terminal of op-amp is zero, the voltage at node 'a' in Fig. 3.7 (a) is v_i same as the input voltage applied to non-inverting input terminal. Now R_f and R_1 forms a potential divider. Hence

$$v_i = \frac{v_0}{R_1 + R_f} R_1$$

$$as\ no\ current\ flow\ into\ the\ op-amp$$

$$\frac{v_o}{v_i} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}$$

Thus, for non inverting amplifier the voltage gain,

$$A_{CL} = \frac{v_o}{v_i} = 1 + \frac{R_f}{R_1}$$

COMPARISON OF THE IDEAL INVERTING AND NON- INVERTING OP-AMPR.

Ideal Inverting amplifier	Ideal non-inverting amplifier
1. Voltage gain=-R_f/R_1	1. Voltage gain=1+R_f/R_1
2.The output is inverted with respect to input	2.No phase shift between input and output
3.The voltage gain can be adjusted as greater than, equal to or less than one	3.The voltage gain is always greater than one
4.The value of input impedance R1 should be kept fairly large to avoid loading effect	4. The input impedance is very large.

3.5 VOLTAGE FOLLOWER:

The lowest gain that can be obtained from a noninverting amplifier with feedback is 1. When the noninverting amplifier is configured for unity gain, it is called a voltage follower because the output voltage is equal to and in phase with the in- put. In other words, in the voltage follower the output follows the input. Although it is similar to the discrete emitter follower, the voltage follower is preferred because it has much higher input resistance, and the output amplitude is exactly equal to the input. To obtain the voltage follower from the noninverting amplifier of Figure 3-2, simply open R, and short RF. The resulting circuit is shown in Fig3.8. In this figure all the output voltage is fed back into the inverting terminal of the op-amp; consequently, the gain of the feedback circuit is 1 (B = A, = 1).

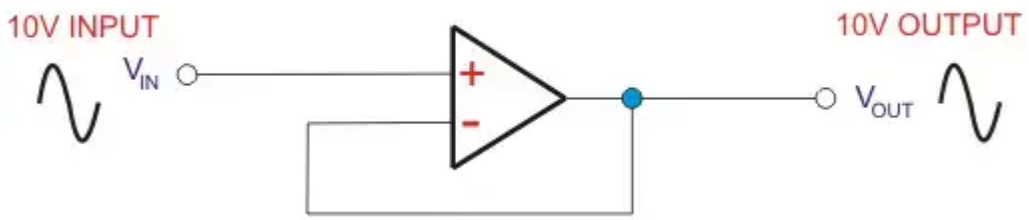

Fig 3.8 Voltage follower

Since the voltage follower is a special case of the noninverting amplifier, all the formulas developed for the latter are indeed applicable to the former except that the gain of the feedback circuit is 1 (B = 1). The applicable formulas are

$$A_F = 1$$

$$R_{iF} = AR_i$$

$$R_{oF} = \frac{R_o}{A}$$

$$f_F = Af_o$$

$$V_{out} = \frac{\mp V_{Sat}}{A}$$

since (1 + A) = A. The voltage follower is also called a noninverting buffer because, when place between two networks, it removes the loading on the first network.

3.6 ADDERS:

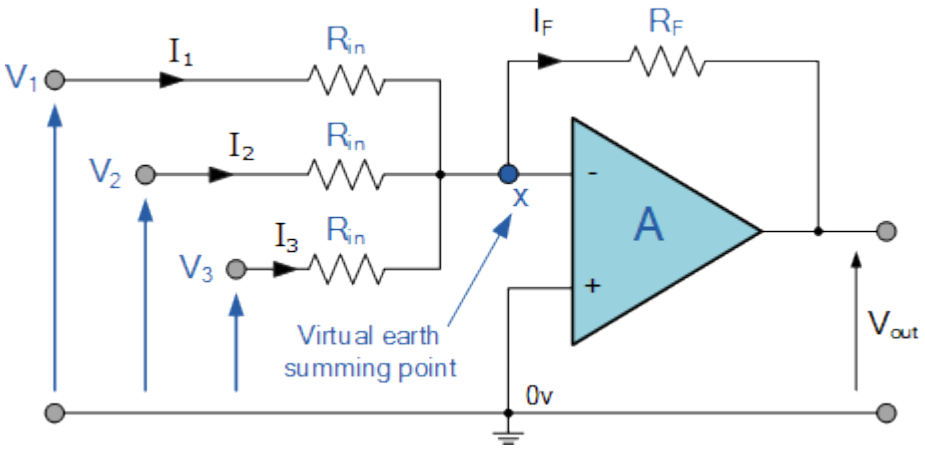

Fig 3.9 Adder

In this simple summing amplifier circuit, the output voltage, (Vout) now becomes proportional to the sum of the input voltages, V_1, V_2, V_3, etc. Then we can modify the original equation for the inverting amplifier to take account of these new inputs thus:

$$I_F = I_1 + I_2 + I_3 = -\left[\frac{V1}{Rin} + \frac{V2}{Rin} + \frac{V3}{Rin}\right]$$

$$\text{Inverting Equation: } Vout = -\frac{Rf}{Rin} \times Vin$$

$$\text{then, } -Vout = \left[\frac{R_F}{Rin}V1 + \frac{R_F}{Rin}V2 + \frac{R_F}{Rin}V3\right]$$

However, if all the input impedances, (R_{IN}) are equal in value, we can simplify the above equation to give an output voltage of:We now have an operational amplifier circuit that will amplify each individual input voltage and produce an output voltage signal that is proportional to the algebraic "SUM" of the three individual input voltages V_1, V_2 and V_3. We can also add more inputs if required as each individual input "sees" their respective resistance, Rin as the only input impedance.This is because the input signals are effectively isolated from each other by the "virtual earth" node at the inverting input of the op-amp. A direct voltage addition can also be obtained when all the resistances are of equal value and R*f* is equal to Rin. Note that when the summing point is connected to the inverting input of the op-amp the circuit will produce the negative sum of any number of input voltages. Likewise, when the summing point is connected to the non-inverting input of the op-amp, it will produce the positive sum of the input voltages.

$$-Vout = \frac{R_F}{R_{IN}}\left(V1 + V2 + V3 \ldots . etc\right)$$

3.7 SUBTRACTOR

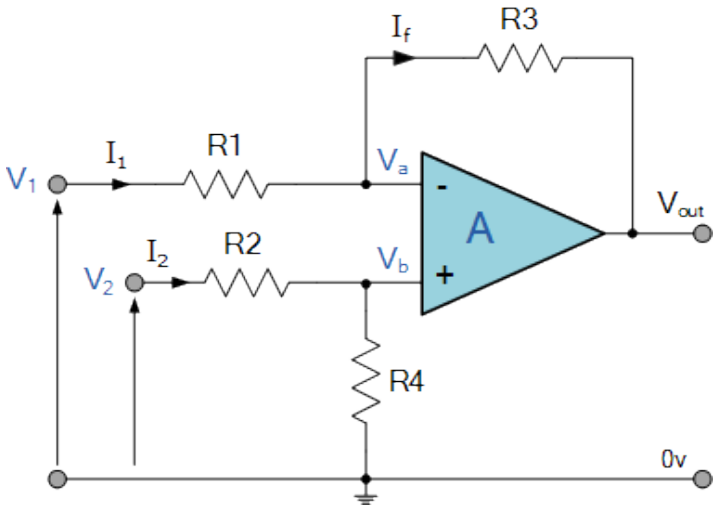

Fig 3.10 Subtractor

By connecting each input in turn to 0v ground we can use superposition to solve for the output voltage Vout. If all the resistors are all of the same ohmic value, that is: R1 = R2 = R3 = R4 then the circuit will become a **Unity Gain Differential Amplifier** and the voltage gain of the amplifier will be exactly one or unity. Then the output expression would simply be Vout = $V_2 - V_1$.

$$I_1 = \frac{V_1 - V_a}{R_1}, \quad I_2 = \frac{V_2 - V_b}{R_2}, \quad I_f = \frac{V_a - (V_{out})}{R_3}$$

$$\text{Summing point } V_a = V_b$$

$$\text{and } V_b = V_2\left(\frac{R_4}{R_2 + R_4}\right)$$

$$\text{If } V_2 = 0, \text{ then: } V_{out(a)} = -V_1\left(\frac{R_3}{R_1}\right)$$

$$\text{If } V_1 = 0, \text{ then: } V_{out(b)} = V_2\left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R_1}\right)$$

$$V_{out} = -V_{out(a)} + V_{out(b)}$$

$$\therefore V_{out} = -V_1\left(\frac{R_3}{R_1}\right) + V_2\left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R_1}\right)$$

Also note that if input V1 is higher than input V2 the output voltage sum will be negative, and if V2 is higher than V1, the output voltage sum will be positive

$$V_{OUT} = \frac{R_3}{R_1}\left(V_2 - V_1\right)$$

3.8 INTEGRATOR:

A circuit in which the output voltage waveform is the integral of the input volt- age waveform is the integrator or the integration amplifier. Such a circuit is ob- tained by using a basic inverting amplifier configuration if the feedback resistor RF is replaced by a capacitor C, The ideal op-amp integrator is an inverting amplifier whose output voltage is proportional to the negative integral of the input voltage thereby simulating mathematical integration.

Operational amplifiers can be used as part of a positive or negative feedback amplifier or as an adder or subtractor type circuit using just pure resistances in both the input and the feedback loop.

But what if we where to change the purely resistive (R*f*) feedback element of an inverting amplifier with a frequency dependant complex element that has a reactance, (X), such as a

Capacitor, C. What would be the effect on the op-amps voltage gain transfer function over its frequency range as a result of this complex impedance.

By replacing this feedback resistance with a capacitor we now have an RC Network connected across the operational amplifiers feedback path producing another type of operational amplifier circuit commonly called an **Op-amp Integrator** circuit as shown below.

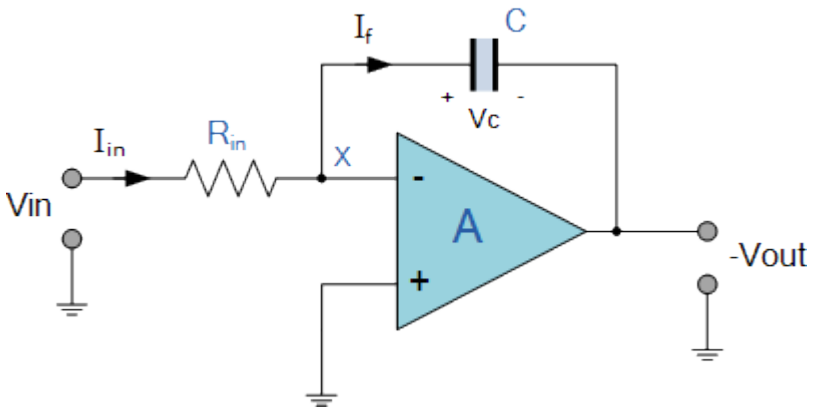

Fig 3.11 Integrator

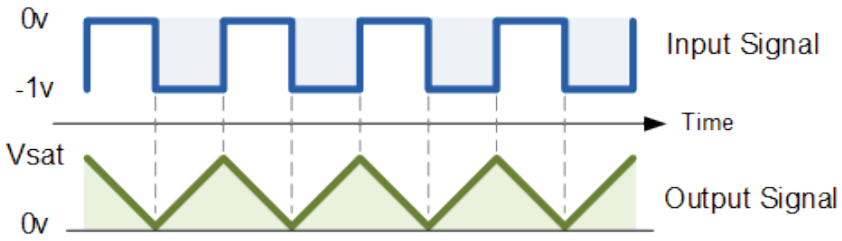

Fig 3.11 Integrator Waveform

We know from first principals that the voltage on the plates of a capacitor is equal to the charge on the capacitor divided by its capacitance giving Q/C. Then the voltage across the capacitor is output Vout therefore: -Vout = Q/C. If the capacitor is charging and discharging, the rate of charge of voltage across the capacitor is given as:

$$V_c = \frac{Q}{C}, \qquad V_c = V_x - V_{out} = 0 - V_{out}$$

$$\therefore -\frac{dV_{out}}{dt} = \frac{dQ}{Cdt} = \frac{1}{C}\frac{dQ}{dt}$$

But dQ/dt is electric current and since the node voltage of the integrating op-amp at its inverting input terminal is zero, X = 0, the input current I(in) flowing through the input resistor, Rin is given as:

$$I_{in} = \frac{V_{in} - 0}{R_{in}} = \frac{V_{in}}{R_{in}}$$

The current flowing through the feedback capacitor C is given as:

$$I_f = C\frac{dV_{out}}{dt} = C\frac{dQ}{Cdt} = \frac{dQ}{dt} = \frac{dV_{out}.C}{dt}$$

Assuming that the input impedance of the op-amp is infinite (ideal op-amp), no current flows into the op-amp terminal. Therefore, the nodal equation at the inverting input terminal is given as:

$$I_{in} = I_f = \frac{V_{in}}{R_{in}} = \frac{dV_{out}.C}{dt}$$

$$\therefore \frac{V_{in}}{V_{out}} \times \frac{dt}{R_{in}C} = 1$$

From which we derive an ideal voltage output for the **Op-amp Integrator** as:

$$V_{out} = -\frac{1}{R_{in}C}\int_0^t V_{in}\,dt = -\int_0^t V_{in}\frac{dt}{R_{in}.C}$$

To simplify the math's a little, this can also be re-written as:

$$V_{out} = -\frac{1}{j\omega RC}V_{in}$$

3.9 DIFFERENTIATOR:

In the differentiator amplifier circuit, the position of the capacitor and resistor have been reversed and now the reactance, X_C is connected to the input terminal of the inverting amplifier while the resistor, R*f* forms the negative feedback element across the operational amplifier as normal.

This operational amplifier circuit performs the mathematical operation of **Differentiation**, that is it "*produces a voltage output which is directly proportional to the input voltage's rate-of-change with respect to time*". In other words the faster or larger the change to the input voltage signal, the greater the input current, the greater will be the output voltage change in response, becoming more of a "spike" in shape.

As with the integrator circuit, we have a resistor and capacitor forming an RC Network across the operational amplifier and the reactance (Xc) of the capacitor plays a major role in the performance of a **Op-amp Differentiator**.

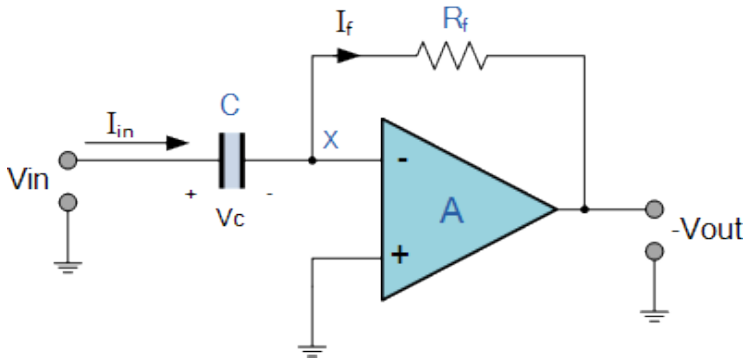

Fig 3.12 Differentiator

The input signal to the differentiator is applied to the capacitor. The capacitor blocks any DC content so there is no current flow to the amplifier summing point, X resulting in zero output voltage. The capacitor only allows AC type input voltage changes to pass through and whose frequency is dependant on the rate of change of the input signal.

At low frequencies the reactance of the capacitor is "High" resulting in a low gain (R*f*/Xc) and low output voltage from the op-amp. At higher frequencies the reactance of the capacitor is much lower resulting in a higher gain and higher output voltage from the differentiator amplifier.

However, at high frequencies an op-amp differentiator circuit becomes unstable and will start to oscillate. This is due mainly to the first-order effect, which determines the frequency response of the op-amp circuit causing a second-order response which, at high frequencies gives an output voltage far higher than what would be expected. To avoid this the high frequency gain of the circuit needs to be reduced by adding an additional small value capacitor across the feedback resistor R*f*.

Since the node voltage of the operational amplifier at its inverting input terminal is zero, the current, i flowing through the capacitor will be given as:

$$I_{IN} = I_F \quad \text{and} \quad I_F = -\frac{V_{OUT}}{R_F}$$

The charge on the capacitor equals Capacitance times Voltage across the capacitor

$$Q = C \times V_{IN}$$

Thus the rate of change of this charge is:

$$\frac{dQ}{dt} = C\frac{dV_{IN}}{dt}$$

but dQ/dt is the capacitor current, *i*

$$I_{IN} = C\frac{dV_{IN}}{dt} = I_F$$

$$\therefore -\frac{V_{OUT}}{R_F} = C\frac{dV_{IN}}{dt}$$

from which we have an ideal voltage output for the op-amp differentiator is given as:

$$V_{OUT} = -R_F C \frac{dV_{IN}}{dt}$$

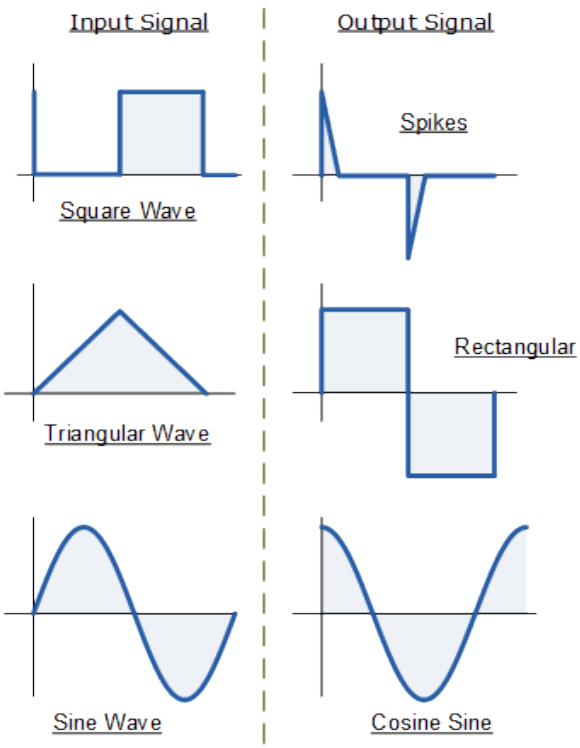

Fig 3.13 Differentiator waveform

3.10 COMPARATOR:

The **Op-amp comparator** compares one analogue voltage level with another analogue voltage level, or some preset reference voltage, V_{REF} and produces an output signal based on this voltage comparison. In other words, the op-amp voltage comparator compares the magnitudes of two voltage inputs and determines which is the largest of the two.

We have seen in previous tutorials that the operational amplifier can be used with negative feedback to control the magnitude of its output signal in the linear region performing a variety of different functions. We have also seen that the standard operational amplifier is characterised by its open-loop gain A_O and that its output voltage is given by the expression: $V_{OUT} = A_O(V+ – V-)$ where V+ and V- correspond to the voltages at the non-inverting and the inverting terminals respectively.

Voltage comparators on the other hand, either use positive feedback or no feedback at all (open-loop mode) to switch its output between two saturated states, because in the open-loop mode the amplifiers voltage gain is basically equal to A_{VO}. Then due to this high open loop gain, the output from the comparator swings either fully to its positive supply rail, +Vcc or fully to its negative supply rail, -Vcc on the application of varying input signal which passes some preset threshold value.

The open-loop op-amp comparator is an analogue circuit that operates in its non-linear region as changes in the two analogue inputs, V+ and V- causes it to behave like a digital *bistable* device as triggering causes it to have two possible output states, +Vcc or -

Vcc. Then we can say that the voltage comparator is essentially a 1-bit analogue to digital converter, as the input signal is analogue but the output behaves digitally.

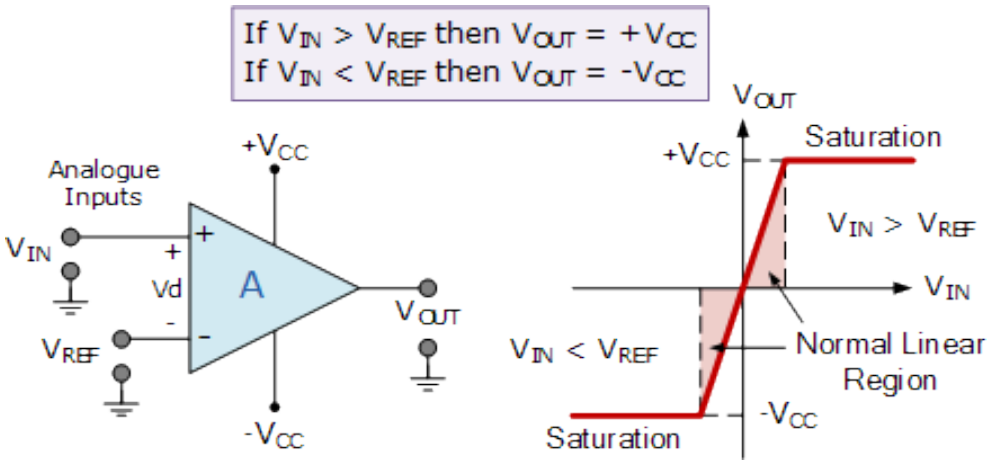

Fig 3.14 Comparator

With reference to the op-amp comparator circuit above, lets first assume that V_{IN} is less than the DC voltage level at V_{REF}, ($V_{IN} < V_{REF}$). As the non-inverting (positive) input of the comparator is less than the inverting (negative) input, the output will be LOW and at the negative supply voltage, -Vcc resulting in a negative saturation of the output.

If we now increase the input voltage, V_{IN} so that its value is greater than the reference voltage V_{REF} on the inverting input, the output voltage rapidly switches HIGH towards the positive supply voltage, +Vcc resulting in a positive saturation of the output. If we reduce again the input voltage V_{IN}, so that it is slightly less than the reference voltage, the op-amp's output switches back to its negative saturation voltage acting as a threshold detector.

Then we can see that the op-amp voltage comparator is a device whose output is dependant on the value of the input voltage, V_{IN} with respect to some DC voltage level as the output is HIGH when the voltage on the non-inverting input is greater than the voltage on the inverting input, and LOW when the non-inverting input is less than the inverting input voltage. This condition is true regardless of whether the input signal is connected to the inverting or the non-inverting input of the comparator.

We can also see that the value of the output voltage is completely dependent on the op-amps power supply voltage. In theory due to the op-amps high open-loop gain the magnitude of its output voltage could be infinite in both directions, (±∞). However practically, and for obvious reasons it is limited by the op-amps supply rails giving V_{OUT} = +Vcc or V_{OUT} = -Vcc.

3.11 SCHMITT TRIGGER

When operating an Op-Amp in the open loop mode, where a feedback is not used, for example, in a Basic Comparator Circuit, the very large open loop gain of the Op-Amp will cause the smallest of noise in the input voltage to trigger the comparator. If the comparator is being used as a Zero Crossing Detector, then such false triggering can cause a lot of problems. It may give a wrong indication of Zero Crossing due to zero crossing of the noise rather than the actual input signals' zero crossing. Schmitt Trigger was invented by Otto Schmitt in early 1930's. It is an electronic circuit that adds hysteresis to the input-output

transition threshold with the help of positive feedback. Hysteresis here means it provides two different threshold voltage levels for rising and falling edge. Essentially, a Schmitt Trigger is a Bi-stable Multivibrator and its output remains in either of the stable states indefinitely. For the output to change from one stable state to other, the input signal must change (or trigger) appropriately. In an Inverting Schmitt Trigger, the input is applied to the inverting terminal of the Op-Amp. In this mode, the output produced is of opposite polarity. This output is applied to non-inverting terminal to ensure positive feedback.

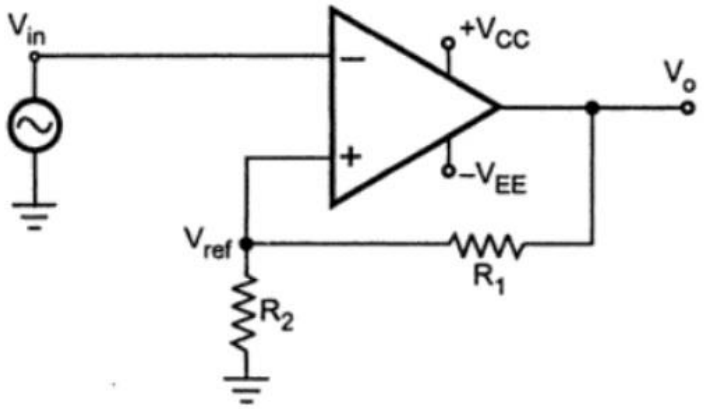

Fig 3.15 Schmitt Trigger

When V_{IN} is slightly greater than V_{REF}, the output becomes $-V_{SAT}$ and if V_{IN} is slightly less that $-V_{REF}$ (more negative than $-V_{REF}$), then output becomes V_{SAT}. Hence, the output voltage V_O is either at V_{SAT} or $-V_{SAT}$ and the input voltage at which these state changes occur can be controlled using R_1 and R_2.

The values of V_{REF} and $-V_{REF}$ can be formulated as follows:

$$V_{REF} = (V_O * R_2) / (R_1 + R_2)$$

But $V_O = V_{SAT}$. Hence,

$$V_{REF} = (V_{SAT} * R_2) / (R_1 + R_2)$$

$$-V_{REF} = (V_O * R_2) / (R_1 + R_2)$$

But $V_O = -V_{SAT}$. Hence,

$$-V_{REF} = (-V_{SAT} * R_2) / (R_1 + R_2)$$

The reference voltages V_{REF} and $-V_{REF}$ are called Upper Threshold Voltage V_{UT} and Lower Threshold Voltage V_{LT}. The following image shows the output voltage versus input voltage graph. It is also known as the Transfer Characteristic of Schmitt Trigger.

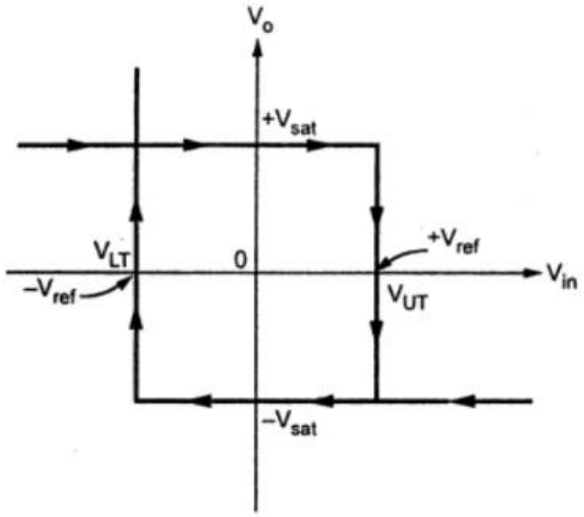

Fig 3.16 Schmitt Trigger transfer characteristic

For a pure sinusoidal input signal, the output of an Inverting Schmitt Trigger Circuit is shown in the following image.

3.12 WEIN BRIDGE OSSCILATOR

Wein Bridge Oscillator is an electronic device that generates sine waves. In the year 1891, Max Wein developed a bridge circuit to measure the impedances. William R.Hewlett designed the Wein-Bridge Oscillator using the Wein bridge circuit and the differential amplifier. Here the Wein bridge is connected in a positive feedback loop between the amplifier output and differential inputs. This can also be viewed as a band-pass filter that provides positive feedback connected to a positive gain amplifier. The bridge circuit is composed of four resistors and two capacitors. The bridge is balanced at the oscillating frequency and has a very low transfer ratio.

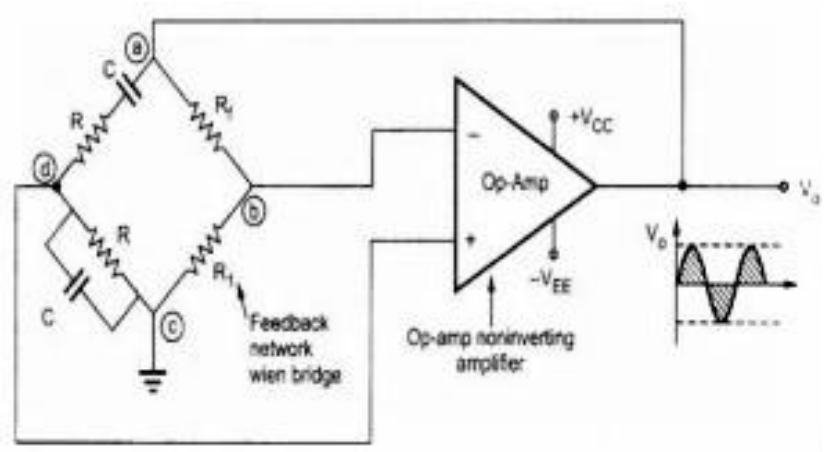

Fig 3.17 Wein Bridge Oscillator

When higher frequencies are applied, the reactance of the capacitors connected in the Wein-bridge is very low. This short circuits the resistor R2 and its output voltage will be zero. At lower frequencies, the higher reactance of the capacitors is observed, and capacitor C1 acts as an open circuit thereby causing the output voltage to be zero. This feature of Wein-bridge observed at the application of lower and higher frequencies, makes it a lead-lag circuit. Here Op-Amp is used as the non-inverting amplifier. The output voltage from the Wein-bridge is fed back to both inverting and non-inverting terminals of the Op-amp.

Advantages of Wein bridge oscillator

1. The overall gain of the oscillator is high as it uses a two-stage amplifier.
2. As no inductors are used in the circuit, there is no issue of interference from external magnetic fields.
3. This oscillator produces a stable sinewave without any distortions.
4. The frequency of the oscillations can be changed by changing the values of capacitors or by the use of a variable resistor in the circuit.
5. The Wein-bridge oscillator has good frequency stability.

Disadvantages of Wein bridge oscillator

1. The two-stage amplifier type of oscillator requires more devices for construction.
2. This oscillator cannot generate very high frequencies, because of the limitations placed on the amplitude and phase-shift values of the amplifier.

Applications:

1. These are highly used for audio testing.
2. Clock signals for testing filter circuits can be generated by this oscillator.
3. Used in distortion testing of power amplifiers.
4. These are also used as excitation for the AC bridges.

3.13 IC-555 TIMER

The 555 Timer, designed by Hans Camenzind in 1971, can be found in many electronic devices starting from toys and kitchen appliances to even a spacecraft. It is a highly stable integrated circuit that can produce accurate time delays and oscillations. The 555 Timer has three operating modes, bistable, monostable and astable mode.

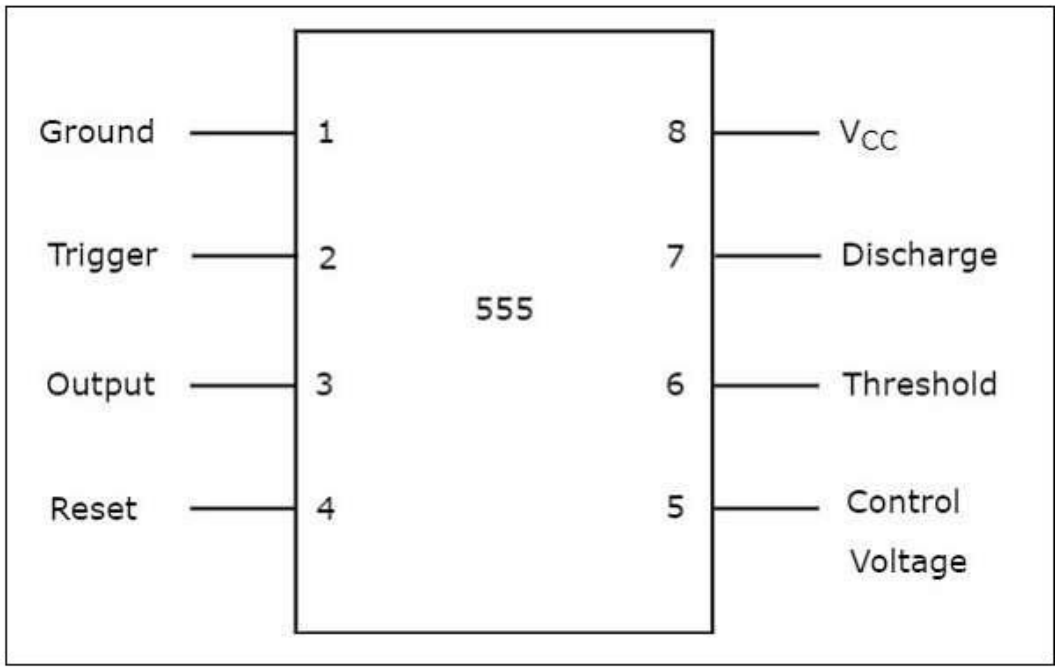

Fig 3.18 IC-555 Pin diagram

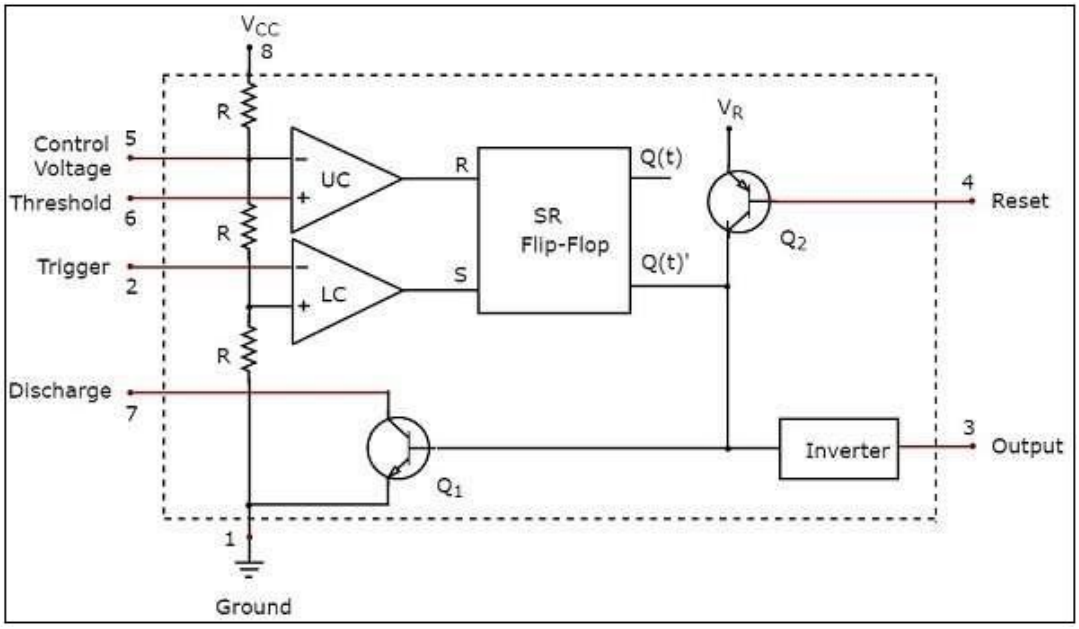

Fig 3.19 IC-555 Internal structure

555 timer is used in almost every electronic circuit today. A 555 timer works as a flip-flop or as a multi-vibrator, it has a particular set of configurations. Some of the major features of the 555 timers would be,

- It operates from a wide range of power ranging from +5 Volts to +18 Volts supply voltage.
- Sinking or sourcing 200 mA of load current.
- The external components should be selected properly so that the timing intervals can be made into several minutes along with the frequencies exceeding several hundred kilohertz.
- The output pin of a 555 timer can drive a transistor-transistor logic (TTL) due to its high current output.
- It has a temperature stability of 50 parts per million (ppm) per degree Celsius change in temperature which is equivalent to 0.005 %/ °C.
- The duty cycle of the timer is adjustable.
- Also, the maximum power dissipation per package is 600 mW, and its trigger pulse and reset inputs have logic compatibility.

3.13.1 ASTABLE OSCILLATOR USING IC 555

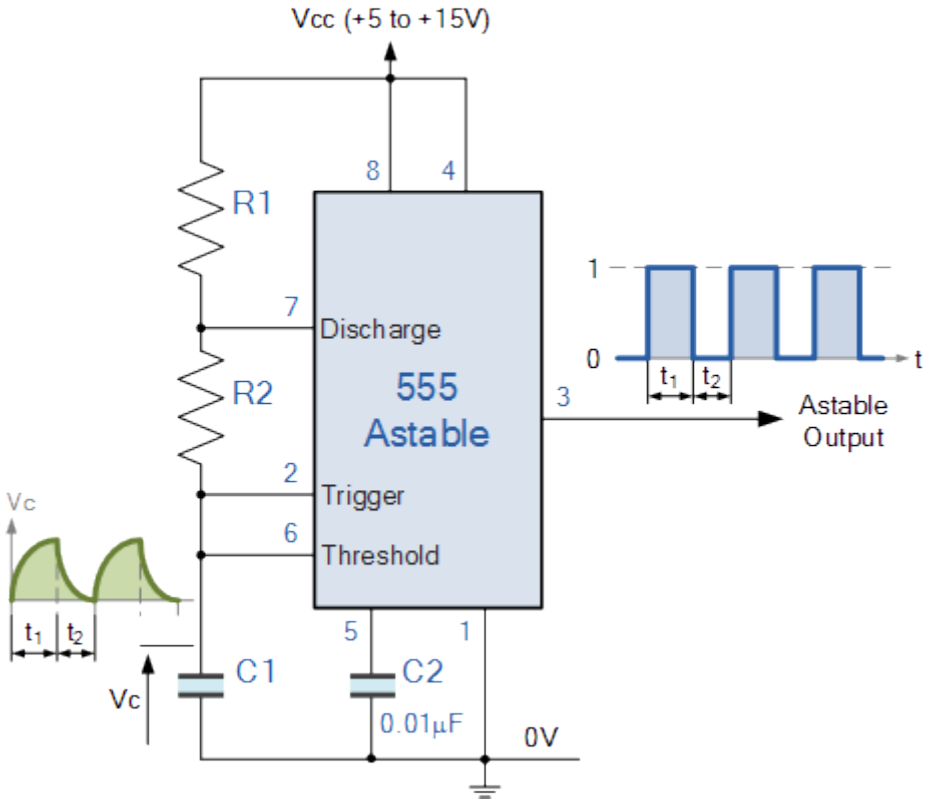

Fig 3.20 Astable multivibrator using IC-555 and waveform

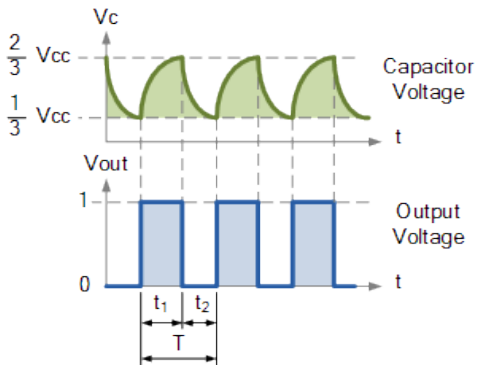

Fig 3.21 Astable multivibrator using IC-555 waveform

In the **555 Oscillator** circuit above, pin 2 and pin 6 are connected together allowing the circuit to re-trigger itself on each and every cycle allowing it to operate as a free running oscillator. During each cycle capacitor, C charges up through both timing resistors, R1 and R2 but discharges itself only through resistor, R2 as the other side of R2 is connected to the *discharge* terminal, pin 7.

Then the capacitor charges up to 2/3Vcc (the upper comparator limit) which is determined by the 0.693(R1+R2)C combination and discharges itself down to 1/3Vcc (the lower comparator limit) determined by the 0.693(R2*C) combination. This results in an output waveform whose voltage level is approximately equal to Vcc – 1.5V and whose output "ON" and "OFF" time periods are determined by the capacitor and resistors combinations. The individual times required to complete one charge and discharge cycle of the output is therefore given as:

Astable 555 Oscillator Charge and Discharge Times

$$t_1 = 0.693(R_1 + R_2).C$$

and

$$t_2 = 0.693 \times R_2 \times C$$

Where, R is in Ω and C in Farads.

When connected as an astable multivibrator, the output from the **555 Oscillator** will continue indefinitely charging and discharging between 2/3Vcc and 1/3Vcc until the power supply is removed. As with the monostable multivibrator these charge and discharge times and therefore the frequency are independent on the supply voltage.

The duration of one full timing cycle is therefore equal to the sum of the two individual times that the capacitor charges and discharges added together and is given as:

555 Oscillator Cycle Time

$$T = t_1 + t_2 = 0.693(R_1 + 2R_2).C$$

The output frequency of oscillations can be found by inverting the equation above for the total cycle time giving a final equation for the output frequency of an Astable 555 Oscillator as:

555 Oscillator Frequency Equation

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2).C}$$

By altering the time constant of just one of the RC combinations, the **Duty Cycle** better known as the "Mark-to-Space" ratio of the output waveform can be accurately set and is given as the ratio of resistor R2 to resistor R1. The Duty Cycle for the 555 Oscillator, which is the ratio of the "ON" time divided by the "OFF" time is given by:

555 Oscillator Duty Cycle

$$\text{Duty Cycle} = \frac{T_{ON}}{T_{OFF} + T_{ON}} = \frac{R_1 + R_2}{(R_1 + 2R_2)} \%$$

The duty cycle has no units as it is a ratio but can be expressed as a percentage (%). If both timing resistors, R1 and R2 are equal in value, then the output duty cycle will be 2:1 that is, 66% ON time and 33% OFF time with respect to the period.

References

1. Ramakanth A Gayakwad, *"Op-Amps and Linear Integrated Circuits"*,4th Edition, Pearson Education, 2022.