AUTONOMOUS

SYLLABUS

VII & VIII Semesters

B.E in Electronics & Communication Engineering

2023

MITE

Invent Solutions

MANGALORE INSTITUTE OF TECHNOLOGY & ENGINEERING

Institute Vision

*"To attain perfection in providing **Globally Competitive Quality Education** to all our Students and also benefit the global community by using our strength in **Research and Development**"*

Institute Mission

*"To establish world class educational institutions in their respective domains, which shall be **Centers of Excellence** in their stated and implied sense. To achieve this objective we dedicate ourselves to meet the challenges of becoming **Visionary and Realistic**, **Sensitive and Demanding**, **Innovative and Practical,** Theoretical **and Pragmatic;** ALL at the same time"*

Department Vision

To emerge as a globally acclaimed centre of learning and innovation in Electronics & Communication Engineering, fostering technically competent, ethical, and innovative engineers through active industry engagement and a commitment to societal advancement.

Department Mission

- *To deliver a flexible curriculum integrated with contemporary academic practices in the field of Electronics & Communication Engineering and emerging technologies, equipping students with in-demand technical competencies.*
- *To provide hands-on learning through technical events, immersive laboratory experiences, industry engagements, and co-curricular activities that bridge academia with real-world engineering challenges.*
- *To instil ethical responsibility, leadership, and community awareness amongst students, preparing them to innovate responsibly and contribute meaningfully to the society.*

Program Educational Objectives (PEOs)

After successful completion of the program, the graduates will be able

- *To produce graduates with strong fundamentals in Electronics & Communication Engineering who can design, implement, and validate systems using modern engineering tools and industry practices.*
- *To enable graduates to thrive in professional roles or higher education pathways, supported by specialized coursework and active industry engagement.*
- *To cultivate lifelong learning, ethical values, and a mindset for research and innovation, enabling graduates to respond to technological evolution and contribute to entrepreneurship and societal development.*

Program Specific Outcomes (PSOs)

At the end of the program, the student will be able to

- *Apply in-depth knowledge of electronics, embedded systems, and semiconductor technologies to analyze, design, and troubleshoot hardware/software integrated systems.*
- *Develop solutions for real-time applications using the principles of communication systems, signal processing, networking, and emerging technologies, complemented by organizational competence and strong ethical values.*

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Autonomous Institute affiliated to VTU, Belagavi, Approved by AICTE, New Delhi
Accredited by NAAC with A+ Grade & ISO 9001:2015 Certified Institution

LIST OF COURSES

VII & VIII Semester Courses			
Sl. No.	**Course Code**	**Course Title**	**Sem**
PROFESSIONAL CORE COURSES			
1.	23ECPC401	ASIC Design	VII
2.	23ECPC402	Digital Image Processing	VII
PROFESSIONAL ELECTIVES COURSES			
3.	23ECPE411	Analog & Mixed Mode VLSI Design	VII
4.	23ECPE412	Wireless Communication	VII
5.	23ECPE413	Wireless Sensor Networks	VII
6.	23ECPE42X	MOOCs (NPTEL/SWAYAM)	VIII
OPEN ELECTIVES COURSES			
7.	23ECOE411	Digital System Design	VII
8.	23ECOE412	Automotive Electronics	VII
9.	23ECOE413	Fundamentals of Wireless Communication	VII
SKILL ENHANCEMENT COURSE			
10.	23ECSE409	Project Phase - II	VII
11.	23ECSE431	Internship	VIII
12.	23ECSE432	Publication / Patenting	VIII
HUMANITIES & SOCIAL SCIENCE COURSE			
13.	23HMCC421	Constitution of India & Professional Ethics	VII

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VII Semester (2023 Scheme): Electronics & Communication Engineering

Sl. No.	Course Code	Course Title	Category	Teaching Dept.	Teaching Hours /Week			Exam Marks			Duration of Exam (SEE) in Hrs	Credits
					L	T	P	CIE	SEE	Total		
1	23ECPC401	ASIC Design	Professional Core	EC	3	0	2	50	50	100	3	4
2	23ECPC402	Digital Image Processing	Professional Core	EC	3	0	2	50	50	100	3	4
3	23ECPE4XX	Professional Elective – III*	Discipline Specific Electives	EC	3	0	0	50	50	100	3	3
4	23ECOE4XX	Open Elective – III**	Open Electives	EC	3	0	0	50	50	100	3	3
5	23ECSE409	Project Phase - II	Skill Enhancement	EC	-	-	12	100	100	200	3	6
6	23HMCC421	Constitution of India & Professional Ethics	Humanities & Social Sciences	Humanities/ Any Department	1	0	0	100	-	100	-	1
										Total Credits		**21**

***Professional Elective Course - III**

Sl. No.	Course Code	Course Title
1	23ECPE411	Analog & Mixed Mode VLSI Design
2	23ECPE412	Wireless Communication
3	23ECPE413	Wireless Sensor Networks

****Open Elective Course - III**

Sl. No.	Course Code	Course Title
1	23ECOE411	Digital System Design
2	23ECOE412	Automotive Electronics
3	23ECOE413	Fundamentals of Wireless Communication

VIII Semester (2023 Scheme): Electronics & Communication Engineering

Sl. No.	Course Code	Course Title	Category	Teaching Dept.	Teaching Hours /Week			Exam Marks			Duration of Exam (SEE) in Hrs	Credits
					L	T	P	CIE	SEE	Total		
1	23ECPE42X	MOOCs* (NPTEL/SWAYAM) 8/12 Weeks	Professional Electives	EC	-	-	-	-	-	100	-	2
2	23ECSE431	Internship	Skill Enhancement	EC	-	-	-	100	100	200	3	12
3	23ECSE432	Publication / Patenting	Skill Enhancement	EC	-	-	-	100	-	100	-	2
										Total Credits		**16**

*** Massive Open Online Courses (MOOCs) -** Identified by the BoS of the department

Guidelines for MOOCs

To promote self-paced, flexible, and industry-relevant learning, a Two-Credit Online professional elective course is introduced in the VIII semester curriculum for all Bachelor of Engineering (B.E.) programs. Students are required to complete an approved online course as per the following guidelines:

1. **Registration and Course Completion:**

   Students must complete any one of the *Board of Studies (BOS)* approved online courses by registering for an 8-week or 12-week course offered through recognized platforms such as NPTEL or SWAYAM. Registration can be done during semester VI or semester VII.

2. **Credit Conversion:**

   The score obtained in the proctored examination conducted by the respective online platform shall be formally converted into course credits as per institute norms.

3. **Provision for students failing to clear the Online Course**

   If a student fails to successfully complete the selected online course within two consecutive attempts before the commencement of Semester VIII, they must register for an elective course offered by the respective department. This elective will be delivered in online mode by the department.

4. **Assessment Pattern for the alternate elective:**

   a. All assignments for the alternate elective course must be submitted online.
   b. The Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE) shall be conducted in offline mode.
   c. Students must physically appear for these examinations at the institute.

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VII & VIII Semesters

ASIC DESIGN			
Semester	**VII**	CIE Marks	**50**
Course Code	**23ECPC401**	SEE Marks	**50**
Teaching Hrs/Week (L: T:P)	**3:0:2**	Exam Hrs	**03**
Total Hrs	**40+24**	Credits	**04**

Course Learning Objectives: This course is designed to

1. Provide an understanding of ASIC types, design flow, and datapath building blocks
2. Familiarize the design-entry techniques and construction methods for ASIC development
3. Introduce the concepts of floorplanning, placement, and routing techniques used in physical design
4. Strengthen the ability to evaluate testability strategies, fault coverage, and scan-based design approaches in VLSI systems

Module 1: Foundations of ASIC and Datapath Logic Cells — **No. of Hrs: 08+04**

Types of ASICs: Full-Custom ASICs, Standard Cell-Based ASICs, Gate Array-Based ASICs, Programmable Logic Devices, Field-Programmable Gate Arrays

Datapath Logic Cells: Datapath Elements, Adders: Carry Skip, Carry Select and Carry Save Adders, Booth Encoding Multipliers, Datapath Operators

Laboratory Component:

To design and verify combinational and sequential circuits used in ASIC datapath elements.(Tool: ncLaunch)

- Half Adder
- Full Adder

Simulate using a testbench

Textbook 1: 1.1, 1.2, 1.5, 2.6.1, 2.6.2, 2.6.4, 2.6.6, 2.7

Module 2: Design Entry and ASIC Construction — **No. of Hrs: 08+04**

Schematic Entry: Hierarchical Design, Cell Library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, Vectored Instances & Buses, Edit in Place, Attributes, Netlist Screener

ASIC Construction: Physical Design, CAD Tools, System Partitioning, Estimating ASIC Size Partitioning Methods: Constructive Partitioning, Iterative Partitioning Improvement, Kernighan-Lin (KL) and Look Ahead Algorithms

Laboratory Component:

To perform RTL synthesis and generate a technology-mapped netlist.(Tool: Genus)

- 4-bit Ripple Carry Adder or 4-bit Counter

Generate reports:

- Area report
- Timing report
- Power estimation

RTL → Gate level conversion

Textbook 1: 9.1, 15.1 to 15.4, 15.7.3, 15.7.4, 15.7.5, 15.7.7

Module 3: Floorplanning and Placement	**No. of Hrs: 08+04**

Goals and Objectives of Floorplanning, Measurement of Delay in Floorplanning, Floorplanning Tools, Channel Definition, I/O and Power Planning, Clock Planning

Goals and Objectives of Placement, Placement Algorithms, Iterative Placement Improvement, Timing Driven Placement Methods, Physical Design Flow

Laboratory Component:

To perform floorplanning and placement for synthesized design. (Tool: Innovus)

Import the netlist generated from Genus.

- Define core area and aspect ratio.
- Define I/O pin placement.
- Create power and ground rings.
- Perform standard cell placement.
- Analyze:
  - Placement density
  - Congestion report

Chip layout planning and placement optimization

Textbook 1: 16.1, 16.2.2, 16.2.4, 16.2.6, 16.2.8, 16.3

Module 4: Routing	**No. of Hrs: 08+06**

Global Routing: Goals and Objectives, Measurement of Interconnect Delay, Global Routing Methods, Global Routing Between Blocks, Global Routing Inside Flexible Blocks, Timing Driven Methods, Back-annotation

Detailed Routing: Goals and Objectives, Measurement of Channel Density, Area-Routing Algorithm, Special Routing: Clock Routing, Power Routing

Laboratory Component:

To implement clock tree synthesis and routing in ASIC design. (Tool: Innovus and STA)
Load placed design.

- Perform Clock Tree Synthesis (CTS).
- Analyze:
  - Clock skew
  - Clock latency
- Run global routing.
- Run detailed routing.
- Verify Design Rule Check (DRC).

Interconnect routing and clock distribution in ASICs

Textbook 1: 17.1, 17.2, 17.2.1, 17.2.2, 17.2.4, 17.2.6, 17.3

Module 5: Design for Testability	**No. of Hrs: 08+06**

Ad hoc Testing, Scan Design: Parallel Scan, Circuit Design of Scannable Elements, Built-in Self-Test (BIST), IDDQ Testing, Design for Manufacturability, Boundary Scan: Test Access Port (TAP), Test Logic Architecture, TAP Controller, Instruction Register, Test Data Registers

Laboratory Component:

1. To implement scan-based design for testability(Tool: Modus)
   - Import synthesized sequential circuit
   - Configure scan chain insertion
   - Convert flip-flops into scan flip-flops
   - Generate scan chains
   - Simulate scan shift operation
   - Generate test patterns
2. Course Project (Complete flow with 8-bit counter design) (RTL to GDSII flow)

RTL Design → Simulation → Synthesis → Floorplan → Placement → CTS → Routing → Scan insertion

Textbook 2: 12.6.1 to 12.6.5, 12.7.1, 12.7.2, 12.7.4, 12.7.5

Course Outcomes: At the end of the course, the student will be able to:

1. **Illustrate** the structure of ASIC design flow, datapath logic units, and testability concepts such as scan and BIST
2. **Outline** the procedures associated with design entry, floorplanning, placement, and routing in ASIC design
3. **Apply** ASIC logic design principles and VLSI testability techniques to improve functional correctness and test efficiency
4. **Use** physical design techniques such as partitioning, floorplanning, placement, and routing to develop optimized ASIC layouts
5. **Apply** ASIC design flow using industry-standard EDA tools to design, synthesize, floorplan, place, route, and test digital circuits for CMOS ASIC implementation

Textbooks:

1. Michael John Sebastian Smith, "Application-Specific Integrated Circuits", 1st Edition, Addison-Wesley Professional, 2025
2. Neil H.E. Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Pearson, 2015

References:

1. Khosrow Golshan, "Physical Design Essentials", 1st Edition, Springer, 2007
2. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits", 3rd Edition, McGraw-Hill, 2003

Web links:

1. VLSI Physical Design, https://onlinecourses.nptel.ac.in/noc21_cs12/preview, IIT Kharagpur
2. VLSI Physical Design with Timing Analysis, https://onlinecourses.nptel.ac.in/noc26_ee90/preview, IIT Roorkee
3. Digital VLSI Testing https://onlinecourses.nptel.ac.in/noc26_ee45/preview, IIT Kharagpur

DIGITAL IMAGE PROCESSING			
Semester	**VII**	CIE Marks	**50**
Course Code	**23ECPC402**	SEE Marks	**50**
Teaching Hrs/Week (L:T:P)	**3:0:2**	Exam Hrs	**03**
Total Hrs	**40+24**	Credits	**04**

Course Learning Objectives: This course is designed to

1. Impart knowledge of Digital Image Processing in perceiving grayscale and color images
2. Familiarize the operation of image enhancement techniques for better image quality
3. Impart skills to apply image restoration methods, compression and mathematical transforms for reconstructing and processing the digital images
4. Introduce and demonstrate the application of frequency-domain techniques, segmentation for analyzing and processing images

Module 1: Digital Image Fundamentals	**No. of Hrs: 08+04**

Introduction to Essential DSP Concepts for Image Processing, Basic Stages of a Digital Image Processing System, Components of an Image Processing System

Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Representing Digital Images

Basic Relationships Between Pixels: Neighbors of a Pixel, Adjacency, Connectivity, Regions, Boundaries

Distance Measures: Euclidian Distance, Chessboard distance, City-Block distance

Linear vs Non linear operations, Arithmetic operations

Laboratory Component:

1. Implement and illustrate pixel distance measures such as Euclidean distance, City-Block distance, and Chessboard distance between selected pixels in a digital image
2. Program to Implement Flip given image horizontally, modify program of horizontal flipping for getting vertical flipping, Perform image arithmetic operation

Textbook 1:1.4, 1.5 ,2.1,2.3 to 2.6.3

Module 2: Image Enhancement	**No. of Hrs: 09+06**

Spatial Domain: Intensity Transformations and Spatial Filtering

Intensity Transformation Functions: Image Negatives, Log Transformation, Power law transformation

Piecewise Linear Transformation: Contrast Stretching, Intensity-Level Slicing, Bit-Plane Slicing

Histogram Processing: Histogram Equalization, Histogram Matching

Fundamentals of Spatial Filtering: Mechanics of Linear Spatial Filtering, Spatial Correlation and Convolution, Vector Representation of Linear Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters
Morphological Operations: Erosion and Dilation, Opening and Closing

Laboratory Components:

1. Program to Implement Power Law Transformation
2. Implement and illustrate Histogram Mapping and Equalization
3. Apply morphological operations such as erosion, dilation, opening, and closing to analyze their effects on binary images

Textbook 1: 3.1 to 3.6, 9.2 to 9.3

Module 3: Image Transforms and Segmentation	**No. of Hrs: 08+06**

Image Transforms: Two-Dimensional DFT, Haar Transform, Discreet Cosine Transform (DCT)
Image Segmentation: Fundamentals, Point Detection, Line Detection, Edge Detection, Edge Linking and Boundary Detection, Thresholding: Global Thresholding, Adaptive Thresholding: Mean, Optimum Global Thresholding Using Otsu's Method

Laboratory Components:

1. Implement the Haar Transform on a digital image and demonstrate image reconstruction using the inverse transform
2. Apply the Discrete Cosine Transform (DCT) to a digital image and illustrate reconstruction from transform coefficients
3. Implement segmentation using Global threshold method

Textbook 2: 5.5, 5.6, 5.9
Textbook 1: 7.1,7.2,10.2,10.3.2,10.3.3

Module 4: Frequency Domain and Color Image Processing	**No. of Hrs: 08+04**

Frequency Domain: Characteristics and fundamentals of Filtering in the Frequency Domain, Image Smoothing and sharpening using Frequency Domain filters.
The Laplacian in the Frequency Domain, Unsharp Masking, High boost Filtering, and High-Frequency-Emphasis Filtering, Homomorphic Filtering
Color Image Processing: Color Fundamentals, Color Models, Intensity Slicing, Intensity to Color Transformations

Laboratory Components:

1. Program to Implement Image Smoothening and Sharpening
2. Apply color image processing techniques including color model conversion, intensity slicing, and intensity-to-color transformation

Textbook 1: 4.7 to 4.9, 6.1 to 6.3

Module 5: Restoration and Compression	**No. of Hrs: 07+04**

Image Restoration: A model of the Image Degradation and Restoration Process, Noise Models, Restoration in the Presence of Noise
Fundamentals of Image Compression Models, Huffman Coding, Golomb Coding, Arithmetic Coding, LZW Coding, Symbol-Based Coding, Bit-Plane Coding

Laboratory Components:

1. Implement image compression using entropy coding techniques such as Huffman coding and Arithmetic coding
2. Implement dictionary-based and bit-plane image compression techniques such as LZW coding and Bit-Plane coding

Textbook 1: 5.1, to 5.3, 8.1,8.2.1-8.2.7

Course Outcomes: At the end of the course, the student will be able to:

1. **Explain** the importance of image processing in perception of gray and color image
2. **Apply** image enhancement techniques and relation between pixels on images
3. **Interpret** image restoration and segmentation techniques on images
4. **Apply** image transformation, techniques, compression and frequency domain filters on digital images
5. **Demonstrate** the application of image processing methods for enhancement, transformation, segmentation, and compression of digital images

Textbooks:

1. Rafael C Gonzalez and Richard E Woods, "Digital Image Processing", 3rd Edition, Pearson, 2018
2. A K Jain, "Fundamentals of Digital Image Processing", 2nd Edition, PHI Learning Private Limited, 2014

References:

1. S Jayaraman, S Esakkirajan, T Veerakumar, "Digital Image Processing", 1st Edition, Tata McGraw Hill, 2014
2. Milan Sonka and Roger Boile, "Image Processing analysis and Machine vision", 4th Edition, Cengage Publications, 2017
3. Rafael C. Gonzalez and Richard E. Woods, "Digital Image Processing Using Matlab"1st Edition, Pearson, 2004
4. Richard Szeliski, "Computer Vision: Algorithms and Applications", 2nd Edition, Springer, 2022
5. Jae S Lim, "Two-Dimensional Image and Signal Processing", Prentice Hall International Edition, 1989
6. Dr. Milindkumar Vinayakrao Sarode, "Digital Image Processing: A Practical approach for Image Restoration", 1st Edition, Lap Lambert Academic Publishing, 2020
7. Khalid Sayood," Introduction to Data Compression" 4th Edition, Morgan Kaufmann Pub, 2012

Web links:

1. Image databases: https://imageprocessingplace.com/root_files_V3/image_databases.htm
2. Student support Materials: https://imageprocessingplace.com/root_files_V3/students/students.htm
3. NPTEL Course, Introduction to Digital Image Processing: https://nptel.ac.in/courses/117105079
4. Computer Vision and Image Processing: https://nptel.ac.in/courses/108103174
5. Image Processing and Computer Vision – Matlab and Simulink: https://in.mathworks.com/solutions/image-video-processing.html

ANALOG & MIXED MODE VLSI DESIGN			
Semester	**VII**	CIE Marks	**50**
Course Code	**23ECPE411**	SEE Marks	**50**
Teaching Hrs/Week (L:T:P)	**3:0:0**	Exam Hrs	**03**
Total Hrs	**42**	Credits	**03**

Course Learning Objectives: This course is designed to

1. Familiarize the fundamental concepts of Metal Oxide Semiconductor (MOS) Device Physics, Single-stage and Differential amplifiers
2. Introduce the concept of Phase Locked Loop (PLLs), and Data Converter architectures used in Mixed Mode VLSI circuits
3. Strengthen the application of MOS Device Models, Amplifier principles while addressing performance trade-offs and device limitations in Mixed Signal VLSI design
4. Impart the ability to design and analyze PLL and Data Converter blocks for given specifications

Module 1: MOS Device Physics and Modeling	**No. of Hrs: 07**
MOS Device Physics: Introduction to Mixed Mode VLSI Design, MOS Device Models, MOS Small Signal Model, MOS SPICE Model, NMOS versus PMOS Devices, Long Channel versus Short Channel Devices Textbook 1: 2.4.1 to 2.4.6	
Module 2: Single Stage MOS Amplifier	**No. of Hrs: 10**
Single Stage Amplifier: Introduction, Common Source (CS) Stage with Resistive Load, CS Stage with Diode Connected Load, CS Stage with Current Source Load, CS Stage with Triode Load, Common Drain, Common Gate Textbook 1: 3.1, 3.2.1 to 3.2.4, 3.3 to 3.4	
Module 3: Differential MOS Amplifier	**No. of Hrs: 09**
Differential Amplifiers: Introduction to Single-ended and Differential Operation, Qualitative Analysis of Basic Differential Pair, Common Mode Response, Differential Pair with MOS Loads, Single Stage Op-Amp Topology Textbook 1: 4.1, 4.2, 4.2.1, 4.3, 4.4, 9.2	
Module 4: MOS Phase-Locked Loop	**No. of Hrs: 08**
Phase Locked Loops: Analysis and Design of PLL, Basic PLL Topology - PLL in Locked condition, Small Transients in Locked condition, Basics of Charge - Pump PLLs, Non-ideal Effects in PLL, Applications Textbook 1:15.1, 15.1.1, 15.1.2, 15.2.3, 15.3.1, 15.3.2, 15.5.1 to 15.5.3	

Module 5: Mixed Signal Data Converter Architectures	**No. of Hrs: 08**
DAC Architecture - Resistor String DAC, R-2R Ladder Networks, Cyclic DAC, Pipeline DAC ADC Architecture-Flash ADC, Two Step Flash ADC, Successive Approximation ADC Textbook 2: 29.1.2, 29.1.3, 29.1.6, 29.1.7, 29.2.1,29.2.2, 29.2.5	

Course Outcomes: At the end of the course, the student will be able to:

1. **Illustrate** the fundamental concepts of MOS device physics and operation of single stage and differential amplifiers in mixed mode VLSI circuits
2. **Outline** the principles of PLL and data converters in mixed mode VLSI design
3. **Apply** MOS device model and amplifier principles in designing mixed signal circuits
4. **Design** PLL building blocks, DAC and ADC architecture for the given specifications

Textbooks:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", 1st Edition, Tata McGraw-Hill, 2002
2. R Jacob Baker, "CMOS Circuit Design, Layout and Simulation", 2nd Edition, Wiley, 2013

References:

1. Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", 3rd Edition, Oxford University Press, 2013
2. Tony Chan Carusone, David A Johns, Kenneth W Martin, "Analog Integrated Circuit Design", 2nd Edition, John Wiley & Sons, 2012
3. Franco Maloberti, "Data Converters", 1st Edition, Springer, 2007

Web links:

1. MOS Small Signal Model: https://youtu.be/YnHAGCGEgxI?si=Du4zii0-zEF3OpZu
2. Common Source Amplifier, Small Signal Analysis: https://youtu.be/jL0BZRhtfCs?si=Drmpt6zVtqKxyENr
3. MOSFET Differential Amplifier: https://youtu.be/9fxcKZls1i8?si=OXqavzd86c_L5C6p
4. OPAMP Design: Basic MOS OPAMP: https://youtu.be/fgmxeWbwupY?si=dmmFKu3eHByo-1S7
5. Data Converters: https://youtu.be/PhTU4pbWMEQ?si=5MdtAu6NiEChpJr2

WIRELESS COMMUNICATION			
Semester	**VII**	CIE Marks	**50**
Course Code	**23ECPE412**	SEE Marks	**50**
Teaching Hrs/Week (L:T:P)	**3:0:0**	Exam Hrs	**03**
Total Hrs	**42**	Credits	**03**

Course Learning Objectives: This course is designed to

1. Introduce the concept of cellular communication and mobile radio propagation for improved performance
2. Introduce the concepts of GSM, CDMA and multicarrier modulation in wireless communication
3. Impart the knowledge on key enablers of LTE 4G and MIMO techniques
4. Design to impart knowledge on performance parameters in mobile communication system

Module 1: Cellular Concept	**No. of Hrs: 08**

The Cellular Concept: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies- Prioritizing Handoffs, Practical Handoff Considerations, Co-Channel Interference and System Capacity, Adjacent Channel Interference, Trunking and Grade of Service, Improving Coverage and Capacity in Cellular Systems: Cell Splitting, Sectoring, Microcell Zone Concept

Textbook 1: 3.1 to 3.4, 3.5.1, 3.5.3, 3.6, 3.7.1, 3.7.2, 3.7.4

Module 2: Mobile Radio Propagation	**No. of Hrs: 08**

Large Scale Path Loss: Free Space Propagation Model, Three Basic Propagation Mechanism- Reflection- Brewster Angle, Reflection From Perfect Conductors, Ground Reflection (Two Ray Model), Diffraction- Fresnel Zone Geometry, Knife-Edge Diffraction Model, Multiple Knife Edge, Scattering- Radar Cross Section Model, Practical Link Budget- Log-Distance Path Loss Model, Log-Normal Shadowing

Textbook 1: 4.2, 4.4, 4.5.2, 4.5.3, 4.6 To 4.8, 4.9.1, 4.9.2, 4.10.1

Module 3: Small Scale Fading and Multipath	**No. of Hrs: 08**

Small Scale Multipath Propagation, Impulse Response Model of a Multipath Channel, Small Scale Multi Path Measurement, Parameters of Mobile Multipath Channels, Types of Small Scale Fading: Fading Effects Due to Multipath Time Delay Spread, Fading Effects Due to Doppler Spread, Diversity and Combining Techniques

Textbook 1: 5.1 to 5.5, 7.10

Module 4: Multiple Access Techniques	**No. of Hrs: 10**
GSM and CDMA System: GSM Network and System Architecture, GSM Channel Concept, TDMA Frames, GSM Identities, CDMA Network and System Architecture - Packet Core Network, CDMA Channel Concept, CDMA Frame Format Key Enablers for LTE 4G: OFDM, Channel Dependent Multiuser Resource Scheduling, Multi-Antenna Techniques, Flat IP Architecture, LTE Network Architecture Multi-Carrier Modulation: Multi Carrier Concepts, OFDM in LTE, OFDM-FDMA, OFDM-TDMA, OFDM-CDMA, OFDMA, SC-FDMA Textbook 2: 5.2 to 5.4, 6.2 to 6.4 Textbook 3: 1.4, 1.5, 3.1, 3.3, 4.1 to 4.3	
Module 5: 5G MIMO system	**No. of Hrs: 08**
5G Architecture: Introduction, NFV Framework, SDN Architecture, RAN Architecture, High-Level Requirements for the 5G Architecture Multiple Input Multiple Output Wireless Communications: Introduction to MIMO Communications, MIMO System Model, MIMO Zero Forcing Receiver, MIMO MMSE Receiver, Singular Value Decomposition of MIMO Channel, Alamouti and Space-Time Codes Textbook 4: 3.1, 3.1.1, 3.1.2, 3.2 Textbook 5: 6.1, 6.2, 6.3, 6.4, 6.8, 6.10	
Course Outcomes: At the end of the course, the student will be able to: 1. **Describe** cellular system design and mobile radio propagation mechanisms in wireless communication systems 2. **Illustrate** the architecture of GSM, CDMA and multicarrier modulation 3. **Describe** key enablers in 4G, 5G architecture and MIMO techniques 4. **Apply** cellular performance parameters in mobile communication system	
Textbooks: 1. Theodore Rappaport, "Wireless Communications: Principles and Practice", 2nd Edition, Pearson Education India, 2018 2. Garry Mullet, "Introduction to Wireless Telecommunication Systems and Networks", 1st Edition, Cengage Learning India Pvt Ltd, 2013 3. Arunabha Gosh, Jun Zhang, Jeffrey G Andrews, Riaz Muhammed, "Fundamentals of LTE", Pearson India Education Services Private Limited, 2018 4. Afif Osseiran, Jose F. Monserrat, Patrick Marsch, "5G Mobile and Wireless Communications Technology", Cambridge University Pres, 2016 5. Aditya K Jagannatham, "Principles of Modern Wireless Communication systems, Theory and Practice", Mc Graw Hill Education (India) Private Limited, 2017	

References:

1. Wei Jiang, Bin Han, "Cellular Communication Networks and Standards: The Evolution from 1G to 6G", Springer Nature, 2024
2. Harri Holma and Antti Toskala, "LTE for UMTS Evolution to LTE Advanced", 2nd Edition, John Wiley & Sons Ltd, 2011
3. T L Singhal, "Wireless Communications", McGraw Hill Education (India) Private Limited, 2016
4. Andreas F. Molisch, "Wireless Communications", 2nd Edition, John Wiley & Sons Ltd, 2011

Web links:

1. Advanced 3G and 4G wireless Mobile communications
   https://nptel.ac.in/courses/117104099
2. Fundamentals of MIMO Wireless Communication
   https://onlinecourses.nptel.ac.in/noc26_ee46/preview

WIRELESS SENSOR NETWORKS			
Semester	**VII**	CIE Marks	**50**
Course Code	**23ECPE413**	SEE Marks	**50**
Teaching Hrs/Week (L:T:P)	**3:0:0**	Exam Hrs	**03**
Total Hrs	**42**	Credits	**03**

Course Learning Objectives: This course is designed to

1. Familiarize the technologies, key issues, and challenges associated with Wireless Sensor Networks (WSN)
2. Describe various architectures, components, standards, and applications of WSN
3. Explain the role of core functional modules in WSN and their contribution toward overall network performance
4. Introduce energy management practices and foundational security mechanisms in WSN

Module 1: Introduction to WSN	**No. of Hrs: 08**

Fundamentals of Wireless Communication Technology, Electromagnetic Spectrum, Radio Propagation, Characteristics of Wireless Channels, Multiple Access Techniques, Overview of WSN, Network Characteristics and Applications, Network Design and Challenges, Differentiating WSNs from MANETs, Technological Background: MEMS, Wireless Communication, Hardware and Software Platform, WSN Standards, Network Architecture, Classification and Protocol Stack for WSN

Textbook 1: 1.1, 1.2, 2.1, 2.2, 2.3, 2.4

Module 2: Medium Access Control (MAC) Protocols	**No. of Hrs: 09**

Introduction and Issues in Designing MAC Protocols, Fundamentals of MAC Protocols, MAC Design for WSN: Network Characteristics, Objectives, Energy Efficiency, Low Duty Cycle Protocols and Wakeup Concepts, Classification of MAC Protocols, MAC Protocols: Contention-Based: S-MAC, DS-MAC, MS-MAC, D-MAC, Sift, T-MAC, Wise MAC, CSMA and MAC with Adaptive Rate Control, Contention-Free and Hybrid protocols, IEEE 802.15.4 MAC protocol

Textbook 1: 3.1, 3.2, 3.3, 3.4

Textbook 2: 5.1 to 5.5

Module 3: Routing Protocols	**No. of Hrs: 09**
Introduction to Routing Protocols, Gossiping and Agent-Based Unicast Forwarding: Randomized Forwarding, Random Walks, Energy-Efficient Unicast: Overview, Multipath Unicast Routing Broadcast and Multicast: Source-Based Tree Protocols, Shared Core-Based Tree Protocols, Mesh-Based Protocols, Geographic Routing: Position-Based Routing, Geocasting, Mobile Nodes: Mobile Sinks, Mobile Data Collectors, Mobile Regions, QoS Based Protocols: Trade-Off Between Energy Saving, Delay, Robustness and Reliability Textbook 1: 4.4.6 Textbook 2: 11.1 to 11.6	
Module 4: Node Clustering, Localization and Data aggregation	**No. of Hrs: 09**
Introduction, Node Clustering Algorithm for WSN: Passive Clustering, Energy–Efficient: Adaptive, Distributed and Hierarchical Clustering, Concepts and Challenges of Node Localization Techniques, Ranging Techniques: TOA and RSS Based Ranging, Wireless Localization Algorithm: Geometrical Triangulation and Pattern Recognition Techniques, Wireless Sensor Node Localization: Cooperative, Centralized and Distributed Localization Algorithm: Introduction and Challenges in Data Aggregation and its Techniques Textbook 1: 6.1, 6.3, 8.1, 8.2, 8.3, 8.4, 8.5, 7.1, 7.3	
Module 5: Energy Efficiency and Security	**No. of Hrs: 07**
Introduction, Need for Energy Efficiency and Power Control, Active and Passive Power Conservation Mechanism, Network Security Introduction: Confidentiality, Integrity, Authenticity, Freshness, Availability, Intrusion Detection and Key Management, Security Issues: Attacks, Defensive Measures Textbook 1: 10.1-10.4, 12.1- 12.9 Textbook 3: 1.2	
Course Outcomes: At the end of the course, the student will be able to: 1. **Explain** the WSN fundamentals, architecture, network characteristics, and standards 2. **Apply** the MAC and routing protocols to ensure effective communication in WSN 3. **Apply** the clustering, localization, and aggregation techniques to optimize network Performance 4. **Illustrate** the energy efficiency techniques and basic security principles in WSN	

Textbooks:

1. Jun Zheng and Abbas Jamalipour, "Wireless Sensor Networks- A Networking Perspective", Wiley-IEEE Press (John Wiley & Sons), 1st Edition, 2009
2. Holger Karl and Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks", John Wiley,1st Edition, 2005
3. Mauro Conti "Secure Wireless Sensor Networks Threats and Solutions", Advances in Information Security, Springer New York, Softcover ISBN: 978-1-4939-4751-5, Published: 23 August 2016

References:

1. C. Siva Ram Murthy, and B. S. Manoj, "AdHoc Wireless networks", Pearson Education, 1st Edition, 2008
2. Feng Zhao and Leonides Guibas, "Wireless sensor networks", Elsevier publication - 2004
3. William Stallings, "Wireless Communications and Networks", Pearson Education - 2004

Web link:

1. "Wireless Ad Hoc and Sensor Networks" by Prof. Sudip Misra (IIT Kharagpur), https://onlinecourses.nptel.ac.in/noc25_cs74/previews

DIGITAL SYSTEM DESIGN			
Semester	**VII**	CIE Marks	**50**
Course Code	**23ECOE411**	SEE Marks	**50**
Teaching Hrs/Week (L:T:P)	**3:0:0**	Exam Hrs	**03**
Total Hrs	**42**	Credits	**03**

Course Learning Objectives: This course is designed to

1. Familiarize learners with the basic concepts of digital logics and systems
2. Impart the knowledge of sequential logics and state machines in digital design
3. Introduce the role of digital system in real world applications

Module 1: Introduction to Digital System	**No. of Hrs: 08**

Introduction, Analog vs Digital systems, Advantages of Digital Systems, Representation of Signals in Digital Form, Signed Number Representation, Arithmetic operations, Binary Coded Decimal, Excess-3 code, Gray code, Code conversion, Parity and Hamming codes

Textbook 1: 1.1, 1.2, 1.3, 2.6, 2.7, 2.10, 2.11, 2.12

Module 2: Boolean Logic and Logic Circuit Design	**No. of Hrs: 08**

Introduction, Boolean algebra, Canonical and Standard forms: Sum of Product (SOP) and Product of Sum (POS), Karnaugh maps, Simplification with Don't Care Conditions, Binary adders: Parallel adder and Carry look ahead adder, Binary subtractors, Magnitude comparators

Textbook 2: 2.1,2.2,2.3,2.5,3.1,3.2,3.3,3.5, 3.8

Module 3: Sequential Logic Circuits	**No. of Hrs: 09**

Introduction, Combinational and Sequential logic, Flip Flops: JK, T, D flip flops, Truth Table and Excitation Tables, Registers, Shift registers, Counters: Asynchronous and Synchronous Counters, Sequence Control in Machines, Event counting and Timing, Logic Families: CMOS Inverter, TTL Inverter, Comparison between CMOS and TTL logic

Textbook 2: 5.1, 5.3

Textbook 1: 8.1, 8.2, 8.3, 8.4, 9.1, 9.2, 9.3, 9.4, 9.5, 11.3, 11.4, 11.6

Module 4: Finite State Machines and Programmable Logic Devices	**No. of Hrs: 09**

Introduction, Concept of Finite State Machine (FSM), Mealy and Moore Models, State diagram, State Table and Reduction, Problem statement to FSM Modeling, Programmable Logic Array (PLA) and Programmable Array Logic (PAL) Architectures, Complex Programmable Logic Device (CPLD) and Field Programmable Gate Array (FPGA)

Textbook 2: 5.4

Textbook 1: 12.1, 12.2, 12.3, 12.8, 12.9

Module 5: Real World Applications	**No. of Hrs: 08**

Introduction, Hard and Soft Real Time Systems, Timing Constraints in Control Applications, Causes of Digital System Failure, Redundancy and Fail-Safe Concepts
Core Avionic Systems, Head-Up Displays, Digital Control and Embedded Systems in CNC Machines and Robotics, And Digital Systems in Industrial Automation
Textbook 3: 1.1, 1.2, 2.1, 2.2
Textbook 4: 1.1, 2.2
Textbook 5: Chapter 4, 5 and 8

Course Outcomes: At the end of the course, the student will be able to:

1. **Explain** fundamental digital logic principles and digital system concepts used in various applications
2. **Explain** the operation and design principles of combinational and sequential digital circuits
3. **Apply** digital logic and sequential circuit concepts to design and implement digital circuit solutions
4. **Describe** the role of digital systems in real-time control, monitoring, and embedded applications

Textbooks:

1. Thomas L Floyd & R.P Jain, "Digital Fundamentals", 8th Edition, Pearson Education, 2015
2. Morris M Mano, "Digital Design", 6th Edition, Pearson Education, 2018
3. Charles H Roth Jr., "Fundamentals of Logic Design", 6th Edition, Cengage Learning,2017
4. R.P.G. Collinson, "Introduction to Avionics systems", Springer Nature, 2023
5. Ranjith Barua, "Robotics, Automation and Computer Numerical Control", 1st Edition, Cambridge Scholars Publication, 2024

Reference:

1. Donald P Leach, "Digital Principles and Applications", 8th Edition, McGraw Hill India, 2014

Web link:

1. Digital system design, IIT, Kharagpur- https://nptel.ac.in/courses/117105080

AUTOMOTIVE ELECTRONICS			
Semester	**VII**	CIE Marks	**50**
Course Code	**23ECOE412**	SEE Marks	**50**
Teaching Hrs/Week (L: T:P)	**3:0:0**	Exam Hrs	**03**
Total Hrs	**42**	Credits	**03**

Course Learning Objectives: This course is designed to

1. Discuss operation of automotive systems/subsystems with emphasis on electronic control integration
2. Explain the functional roles of control components in embedded system design for various automotive applications
3. Describe automotive networks, diagnostic methodologies, and standards along with the emerging vehicle technologies

Module 1: Introduction and Engine Control	**No. of Hrs: 09**
Evolution And Need of Automotive Electronics, Physical Configuration, Engine, Electronic Control Unit (ECU): ECU Block Diagram, Design Cycle (V Model), Engine Control, Electronic Engine, Control: Subsystems, Engine Performance Terms, Mapping, Effect Of Air/Fuel Ratio, Exhaust Gas Recirculation (EGR) Textbook 1: Chapter1, Chapter 5	
Module 2: Control Components	**No. of Hrs: 08**
Automotive Sensors: Variables, Airflow Rate, Manifold Absolute Pressure (MAP), Position, Crankshaft Position, Throttle Angle, Temperature, Oxygen, Knock, Vision Perception Sensors and Sensor Fusion Techniques, Actuators: Solenoid, Fuel Injector, Variable Valve Timing (VVT) Actuator, Ignition System Textbook 1: Chapter 6	
Module 3: Electronic Architecture and Applications	**No. of Hrs: 09**
Overview, Vehicle System Architecture, Electronic Architecture: Distributed Ecus, Domain Controllers, Centralized Vehicle Architecture, Functional Structure, Cruise Control System, Traction Control, Anti-Lock Braking System (ABS), Safety Systems, Infotainment and Vehicle Multimedia, Driver Assistance & Navigation Textbook 1: Chapter 8 Textbook 2: Pg. 152-161	
Module 4: Networking, Diagnostics and Standards	**No. of Hrs: 08**
Communication Interfaces, Automotive Networking: Bus Stem- Classification, Applications in the Vehicle, Coupling of Networks, Buses (CAN, LIN, Flex Ray, MOST, Ethernet), Diagnostic Interfaces, Unified Diagnostic Service (UDS), Automotive Diagnostics, Functional Safety Textbook 2: Pg. 85-151 Textbook 1: Chapter10	

Module 5: Future Electronic Systems	**No. of Hrs: 08**
Future Automotive Electronic Systems: Collision Avoidance Radar Warning Systems, Low Tyre Pressure Warning Systems, Radio Navigation, Signpost Navigation, Dead Reckoning Navigation, Voice Recognition, Telematics, Stability Augmentation, Connected Vehicles Textbook 1: Chapter 11	

Course Outcomes: At the end of the course, the student will be able to:

1. **Describe** the architecture and operation of automotive systems and components, with focus on electronic control integration
2. **Design** electronic control systems integrating automotive components and network frameworks
3. **Review** emerging automotive technologies, networks, diagnostic, and standards

Textbooks:

1. William B Ribbens, "Understanding Automotive Electronics", 6th Edition, Butterworth–Heinemann (Elsevier), 1998
2. Robert Bosch GmbH (Ed.), "Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive", 5th Edition, John Wiley & Sons Inc., 2007
3. Functional Safety standards ISO 26262, white papers

References:

1. Bosch Automotive Handbook, 11th Edition, 2022
2. Denton "Automobile Electrical and Electronic Systems", 5th Edition, Routledge, Taylor Francis, 2017
3. David Hoyle "Automotive Quality systems", Butterworth Heinemann limited, 2015
4. Nicholas Navet "Automotive Embedded System Handbook", CRC Press, 2009
5. Mitchell, Harvey B. "Multi-Sensor Data Fusion: An Introduction". Springer Science & Business Media, 2007

Web links:

1. "Fundamentals of Automotive Systems", Prof. C. S. Shankar Ram, IITM, https://nptel.ac.in/courses/107106088
2. "Automotive Electrics and Automotive Electronics", https://www.udemy.com/course/automotive-electrics-and-automotive-electronics

FUNDAMENTALS OF WIRELESS COMMUNICATION			
Semester	**VII**	CIE Marks	**50**
Course Code	**23ECOE413**	SEE Marks	**50**
Teaching Hrs/Week (L:T:P)	**3:0:0**	Exam Hrs	**03**
Total Hrs	**42**	Credits	**03**

Course Learning Objectives: This course is designed to

1. Introduce the evolution of wireless radio and communication systems
2. Introduce the structure of a GSM mobile handset and the key operational procedures involved in cellular communication
3. Impart the knowledge of wireless modulation techniques
4. Familiarize the wireless networking standards

Module 1: Fundamentals of GSM Mobile Systems	**No. of Hrs: 08**

Evolution of Wireless Radio Systems, Wireless Communication Systems: Cordless Telephone Systems, Cellular Telephone Systems
GSM Mobile Handset: Introduction to the GSM Handset, Functional Blocks Inside a GSM Mobile Phone, Hardware Block Diagram of a Mobile Phone, GSM Transmitter and Receiver Module, Subscriber Identity Module (SIM)
Textbook 1: 1.1,1.4
Textbook 4: 10.1,10.2,10.3,10.4,10.11

Module 2: GSM Network Operations and Mobility Management	**No. of Hrs: 10**

Initial Procedures after Mobile Power ON, Idle Mode, Location Updating, Security Procedure, Access Mode, Handover, Radio Resource Control Procedure, Mobility Management Procedure, Call Routing, Power Control
Textbook 4: 9.1 to 9.10

Module 3: Cellular Systems and Modulation Techniques	**No. of Hrs: 08**

Cellular Concept, Cell Fundamentals, Capacity Expansion Techniques - Cell Splitting, Cell Sectoring, Wireless Telecommunications Coding Techniques, Digital Modulation Techniques, Spread Spectrum Modulation Techniques, Diversity Techniques
Textbook 2: 4.1 to 4.3, 8.3,8.4,8.5,8.7

Module 4: Broadband Wireless Access Technologies	**No. of Hrs: 08**

Introduction To Wireless LAN 802.11X Technologies, Evolution of Wireless LANs, Introduction To 802.15x Technologies, Wireless PAN Applications And Architecture, Introduction To Broadband 802.16x Technologies, Wireless MANs
Textbook 2: 9.1, 9.2, 10.1,10.2, 11.1,11.2

Module 5: Evolution of Cellular Technologies	**No. of Hrs: 08**

Introduction, Evolution of Mobile Broadband: First Generation Cellular Systems, 2G Digital Cellular Systems, 3G Broadband Wireless Systems, Beyond 3G: HSPA+, Wimax, And LTE, Key Enabling Technologies And Features Of LTE, OFDM, SC-FDE And SC-FDMA, Multi Antenna Techniques, LTE Network Architecture, Future Of Mobile Broadband - Beyond LTE
Textbook 3: 1.1, 1.2,1.4, 1.5, 1.7

Course Outcomes: At the end of the course, the student will be able to:

1. **Illustrate** the evolution of wireless radio systems, architecture and functional blocks of a GSM mobile handset
2. **Describe** the procedures involved in mobile power ON, idle mode operation, location updating, and basic mobility management in cellular communication systems.
3. **Describe** the cellular concepts, capacity enhancement methods, modulation techniques and wireless network access technologies in wireless communication.
4. **Apply** the channel capacity expansion and modulation techniques, power control techniques on system performance in the wireless communication system

Textbooks:

1. Theodore Rappaport, "Wireless Communications: Principles and Practice", 2nd Edition, Pearson Education India, 2017
2. Garry Mullet, "Introduction to Wireless Telecommunication systems and Networks", 1st Edition, Cengage Learning India Pvt Ltd, 2013
3. Arunabha Gosh, Jun Zhang, Jeffrey G Andrews, Riaz Muhammed, "Fundamentals of LTE", Pearson India Education Services Private Limited, 2018
4. Sajal Kumar Das, "Mobile Handset Design", John Wiley & Sons (Asia) Pte Ltd, 2010

References:

1. T L Singhal, "Wireless Communications", McGraw Hill Education (India) Private Limited, 2016
2. Andreas F. Molisch, "Wireless Communications", 2nd Edition, John Wiley & Sons Ltd, 2011
3. Aditya K Jagannatham, "Principles of Modern Wireless Communication systems, Theory and Practice ", Mc Graw Hill Education (India) Private Limited, 2017
4. Jochen Schiller, "Mobile Communications", 2nd Edition, Pearson Education, 2019

Web link:

1. Introduction to Wireless and Cellular Communications: https://nptel.ac.in/courses/106106167

PROJECT PHASE – II			
Semester	**VII**	CIE Marks	**100**
Course Code	**23ECSE409**	SEE Marks	**100**
Teaching Hrs/Week (L:T:P)	**0:0:12**	Credits	**06**

Objectives:

1. To enable students to execute, validate, and communicate the engineering solution to the identified problem conceptualized in Project Phase – I
2. To motivate students to extend their project work toward research publications, patent filing, funding proposals, or technology transfer, where applicable

General Guidelines for CIE procedure:

1. The Department project coordinator will take the responsibility of monitoring all the activities related to the project execution.
2. The HOD shall constitute project evaluation/review committee(s) & the composition shall be as follows:
    a. HOD or one of the HODs in case of an interdisciplinary project, shall be the Chairman of the committee
    b. Project Coordinator shall be member - Convener
    c. Project guide shall be the member
    d. One/Two senior faculty members nominated by the HOD (may be from different departments in case of an interdisciplinary project jointly nominated by the HODs)
3. Project teams must implement the problem identified using the proposed methodology through systematic experimentation and/or simulation leading to a functional solution or validated outcome in consultation with their project guide.
4. Each project team shall maintain a project diary and record their project progress at regular interval of time. This shall carry signature of the students and the project guide.
5. Marks may be equally or proportionally distributed among team members based on contribution assessed by the guide and committee.
6. A student shall obtain minimum of 40% of the total CIE marks to gain eligibility for SEE

General Guidelines for SEE procedure:

1. The Department project coordinator will take the responsibility of all the requirements for successful conduction of the SEE.
2. SEE for project work will be conducted by two examiners (one internal examiner and the other an external examiner) appointed by the Controller of Examinations.
3. Project teams must present their projects that have been executed and completed with a functional solution or validated outcome during the SEE.
4. Each project team shall bring to the SEE a project report that shall carry signature of the students, project guide, HOD and the Principal. Plagiarism, data fabrication, or copying of work will result in stringent disciplinary action and /or penalties. (Note: Any disciplinary actions or penalties will be as per institutional policy.)
5. Marks may be equally or proportionally distributed among team members based on contribution assessed by the examiners.
6. A student shall obtain minimum of 40% of the total SEE marks to pass this course.

Deliverables:

1. Comprehensive Project Report comprising of:
    - Abstract
    - Introduction
    - Literature Survey
    - Problem Definition
    - Proposed Methodology
    - Design
    - Implementation
    - Results and discussion
    - References
    - Appendices

   The project report shall be prepared in the prescribed format provided by the institute.
2. A plagiarism report shall be obtained from the Department of Library. Acceptable similarity threshold is generally below 20%, and hence, the plagiarized content shall not exceed 20%. Similarity above 20% will require resubmission after proper revisions.

Review and Evaluation for CIE:

1. There shall be two reviews and a presentation. Total of 100 CIE marks is distributed as follows:

Review - 1	
Phase wise execution of proposed solution	20 Marks
Use of modern tools for proposed solution	10 Marks
Contribution as an individual and team member	10 Marks
Total	**40 Marks**
Review - 2	
Complete Implementation and Demonstration of Modules	15 Marks
Report Quality & Formatting	15 Marks
Total	**30 Marks**
Presentation	
Presentation	20 Marks
Team work	10 Marks
Total	**30 Marks**

Grand Total	**100 Marks**

2. First review shall be conducted after one month from the start of the semester
3. Every department shall develop rubrics to assess performance of the students based on the above given parameters

Evaluation for SEE:

1. There shall be a presentation for SEE. Total of 100 SEE marks is distributed as follows:

SEE	
Execution of proposed solution	40 Marks
Evaluation of Project Report	30 Marks
Project presentation & Question and Answer	30 Marks
Total	**100 Marks**

Course Outcomes: At the end of the course, the student will be able to:

1. Execute the problem identified using the methodology proposed through systematic design, development, experimentation, and/or simulation, leading to a functional solution or validated outcome
2. Translate theoretical concepts into practical implementation while considering constraints such as feasibility, cost, sustainability, safety, ethics, and societal relevance
3. Exhibit the resourcefulness to act independently as well as collaboratively within a team in overcoming technical challenges encountered during project execution
4. Plan tasks effectively, manage time and resources, meet defined milestones, and adhere to deadlines, reflecting professional engineering practice
5. Prepare a comprehensive project report that clearly documents design decisions, implementation details, experimental results, analysis, and conclusions using standard technical writing practices
6. Confidently present the project work through reviews, demonstrations, seminars, and viva-voce examinations, addressing questions from peers, faculty, and examiners

CONSTITUTION OF INDIA & PROFESSIONAL ETHICS			
Semester	**VII**	CIE Marks	**100**
Course Code	**23HMCC421**	SEE Marks	**-**
Teaching Hrs/Week (L:T:P)	**1:0:0**	Exam Hrs	**-**
Total Hrs	**13**	Credits	**01**

Course Learning Objectives: This course is designed to

1. Introduce the foundational principles and features of the Indian Constitution
2. Familiarize the Fundamental Rights and Directive Principles
3. Provide an understanding of Union and State government policies and Electoral Process
4. Develop awareness on Sustainable development goals, energy conservation and climate change
5. Inculcate Ethical responsibilities and Code of Conduct

Module 1: Introduction to the Indian Constitution	**No. of Hrs: 02**

Definition and Significance of the Constitution, Making of the Constitution, Constituent Assembly, Preamble, Salient features of the Indian Constitution, Amendments, Schedules and Citizenship

Module 2: Fundamental Rights and Duties	**No. of Hrs: 04**

Fundamental Rights: Right to Equality, Right to Freedom, Right to Life & Personal Liberty, Right against Arbitrary arrest and Preventive Detention, Right against Exploitation, Right to Religion, Cultural & Educational Rights and Right to Constitutional Remedies, Restrictions and Limitations, Directive Principles of State Policy and its relevance in society, Fundamental Duties of Citizens

Module 3: Union and State Government Structure	**No. of Hrs: 03**

Union Govt: Union Legislature- Parliament-Lok Sabha and Rajya Sabha, Sessions of Parliament, Parliamentary System, Parliamentary Committees, Important Parliamentary Terminologies, Union Executive– President, Prime Minister, Union Cabinet, Union Council of Ministers, Union Judiciary-Supreme Court of India, Judicial Review and Judicial Activism State Govt: State Legislature- State Legislative Assembly, State Legislative council, State Executive- Governor, Chief Minister, State Cabinet, State Council of Ministers, State Judiciary- High Court and Subordinate Courts, Elections: Election Commission of India, Process and Laws, Emergency Provisions

Module 4: Ethics and Sustainable Development	**No. of Hrs: 02**

Ethics: Values and types, Honesty, Trust, Integrity and Reliability in Engineering, Sustainable development goals, energy conservation, sustainable developments, Environmental Ethics: climate change and ethical responsibility

Module 5: Professional Ethics for Engineers	**No. of Hrs: 02**
Scope & Aims, Code of Ethics, Professional responsibility, Accountability, Research Ethics, Clash of Ethics (example with respect to technology), Conflicts of Interest, Risks, Safety, Liability and Corporate Social Responsibility	

Course Outcomes: At the end of the course, the student will be able to:

1. **State** the preamble and the basic features of the Indian Constitution
2. **Explain** the Fundamental Rights, Directive Principles of State Policy and their relevance in contemporary Indian society
3. **Compare** the functioning of the Union and State legislature, Executive and Judiciary
4. **Classify** Ethical, Virtues and explain sustainable development goals and climate change
5. **Outline** the Aims, Code of Ethics, and principles of Corporate Social Responsibility

Textbooks:

1. Raja Ram, M., "Constitution of India & Professional Ethics", 3rd Edition, New Age International Publishers, 2015
2. Dr. Tharanath, Santhosh Prabhu, Suma Suresh Kogilgeri, "Constitution of India & Professional Ethics", Pristine Publishing House, 2018
3. Brij Kishore Sharma, "Introduction to the Constitution of India", 8th Edition, PHI Learning Pvt. Ltd., 2011
4. Charles E. Harris, Michael S. Pritchard, Michael J. Rabins, "Engineering Ethics: Concepts and Cases", 1st Edition, IEEE / Cengage, 2018
5. Jaquir Iqbal, "SDG – Sustainable Urban Development: Challenges, Achievements & Opportunities", 1st Edition, Global Vision Publishing House, 2013

Web links:

1. Making of the Indian Constitution - https://www.youtube.com/watch?v=Z5nQ4xea9ts
2. Parts, Articles and Schedules of the Indian Constitution - https://www.youtube.com/shorts/TJRdYarLPYI
3. The Indian Constitution - https://www.youtube.com/watch?v=vXvlSXlmkyM
4. Professional Engineering Ethics - https://www.youtube.com/watch?v=SVz6Q7EoBJM
5. Sustainable Development Goals- https://www.youtube.com/watch?v=qAIolKgDPrA

INTERNSHIP			
Semester	**VIII**	CIE Marks	**100**
Course Code	**23ECSE431**	SEE Marks	**100**
Teaching Hrs/Week (L:T:P)	**-**	Exam Hrs	**03**
Total Hrs	**-**	Credits	**12**

Objectives:

1. Bridge the gap between academic learning and real-world engineering practice
2. Provide hands-on experience in industry, research and incubation environments
3. Develop technical, analytical, and professional skills
4. Expose students to organizational structure, workflow, and workplace ethics
5. Enhance employability, innovation, and lifelong learning capabilities

Preamble:

Internship refers to the position of a student as trainee or a temporary (or unconfirmed) employee, who works in an organization, with or without pay/stipend, in order to gain work experience or satisfy requirements for a qualification. It is a structured, supervised professional experience in an industry, research organization, or incubation centers

Internships play a vital role in bridging the gap between theoretical education and professional practice. In general, engineering internships serve as a crucial component of professional education by providing experiential learning, industry readiness, and holistic skill development, ultimately producing competent engineers or entrepreneurs. Apart from these, it develops professional ethics, work culture awareness and communication skills

Types of Internships:

Following are the types of internships:

i. **Industry Internship**: Carried out in the engineering industry, companies, manufacturing units, startups, business, IT industry. The topic involved may be technical, managerial, production-related tasks, live projects, or innovative activities

ii. **Research Internship**: Carried out at universities, research labs, or R&D departments or organizations. The internship involves literature review, data analysis, and experimental work leading to publications, prototypes, technical reports or innovations. The research internship may induce students to plan for higher studies or academic careers

iii. **Entrepreneurship Internship**: Undertaken in association with start-ups, or entrepreneurship cells or launching own idea in Preincubation/Incubation centers.

The internship offers exposure to business planning, prototype, product development, and promotes innovation, risk-taking, and entrepreneurial mindset

iv. **Post-Placement Internship**: Refers to the internship offered to students after they receive a confirmed job offer (placement) from a company, but before formally joining as full-time employees. This internship (on-site, virtual, or hybrid) ensures that students are groomed to be professionally ready, technically competent, and culturally aligned with the organization even before official induction

General Guidelines:

1. The official engagement period of 15-week for students selected/recruited by the company/ organization only at their premises under the supervision of the company, shall only be considered as an internship
2. The period of training and working of students who have been recruited as employees by organizations at the beginning of the 4th year of the program, shall also be treated as an internship
3. The assigned faculty mentor/coordinator/guide should monitor the student's progress, and document offer letters, training reports, attendance, and evaluations for awarding academic credits
4. All students undergoing an internship, should adhere to all the guidelines, reporting protocols, and evaluation procedures prescribed by the Institution and the company.
5. Students must submit the certificate of completion of an internship with the period of internship clearly mentioned, from the respective company/organization

Procedure for CIE:

1. The Department Internship coordinator identified by the HOD will take the responsibility of monitoring all the activities related to the Internship.
2. The HOD shall constitute Internal Internship evaluation/review committee & the composition shall be as follows:
    a. HOD shall be the Chairman of the committee
    b. Internship Coordinator shall be member – Convener
    c. Internal Internship Guide shall be member
    d. Two senior faculty members nominated by the HOD shall be the members

3. The External Internship evaluation/review committee shall be composed of industry supervisor/external guide. For evaluation, the industry supervisor/external guide may join the review in online mode
4. The internal evaluation shall be conducted by the departmental review committee based on the student's internship progress, documentation, and presentation which will comprise the student's daily report, focusing on the regularity, completeness, and clarity of the internship logbook/diary; the deliverables and outcomes, considering the quality of work, relevance, and achievement of the stated objectives; and the presentation skills, assessing clarity, communication effectiveness, and the ability to present the work in a structured and professional manner
5. The external evaluation shall be carried out by the industry supervisor/external guide based on the student's performance at the workplace which will comprise the student's technical knowledge, assessment of the understanding and application of domain-specific concepts during the internship; work ethics, considering professionalism, punctuality, discipline, and adherence to organizational practices; deliverables and outcomes, evaluating the quality and completion of assigned tasks; and the ability to learn independently, adapt to new and emerging technologies, and exhibit critical thinking, reflecting the student's capacity for continuous learning, problem-solving, and adaptability in a professional environment

Procedure for SEE:

1. SEE for Internship will be conducted by two examiners (one internal examiner and the other an external examiner) appointed by the Controller of Examinations
2. Students must present their Internship work to the examiners
3. Each student shall bring to the SEE, an Internship report which includes the Internship Completion Certificate from the organization. The report shall also carry signatures of the student, Internship guides (Internal & External), HOD and the Principal

Deliverables:

1. Internship Daily Report
2. Final Internship Report
3. Internship Completion Certificate

Evaluation for CIE:

There shall be two reviews and a presentation. Total of 100 CIE marks is distributed as follows:

Review – 1 & 2 (Internal Internship Evaluation Committee)	
Internship Daily Report	10 Marks
Deliverables and Outcomes	10 Marks
Presentation Skills	05 Marks
Review – 1 Total	**25 Marks**
Review – 2 Total	**25 Marks**
Review – 1 & 2 (External Internship Evaluation Committee)	
Technical Knowledge	10 Marks
Work Ethic	05 Marks
Deliverables and Outcomes	05 Marks
Ability to Learn, Adapt & Critical Thinking	05 Marks
Review – 1 Total	**25 Marks**
Review – 2 Total	**25 Marks**
Grand Total	**100 Marks**

Evaluation for SEE:

Total of 100 SEE marks is distributed as follows:

SEE (Internal & External Examiners)	
Internship Report	70 Marks
Final Presentation	30 Marks
Grand Total	**100 Marks**

Course Outcomes:

At the end of the course, the student will be able to:

1. Apply engineering knowledge to real-world industrial or societal problems
2. Demonstrate technical competency in a professional environment
3. Analyze and solve practical engineering problems using modern tools / techniques

4. Communicate effectively through reports and presentations
5. Exhibit professional ethics, teamwork, and adaptability
6. Inculcate industry practices, workflows, and organizational behavior

PUBLICATION / PATENTING			
Semester	**VIII**	CIE Marks	**100**
Course Code	**23ECSE432**	SEE Marks	**-**
Teaching Hrs/Week (L:T:P)	**-**	Exam Hrs	**-**
Total Hrs	**-**	Credits	**02**

Objectives:

1. Enable students to systematically document literature review and research gaps
2. Train students in research paper writing and publication process
3. Provide knowledge of patentability search and drafting patent applications
4. Motivate students to publish research work or file patents
5. Inculcate ethical research practices

Procedure for CIE:

1. The project guide from Project Phase I / II shall continue as the research guide, ensuring continuity in converting the completed project work into a research publication or patent.

2. Students shall derive research contributions from their completed project work, focusing on:
   a. Accurately representing experimental results
   b. Providing evidence for validated outcomes / effective performance
   c. Explicit mention of novelty / innovation

3. The evaluation shall be carried out based on the following three major components:
   Component 1: Literature Review & Manuscript / Patent Drafting
   a. Comprehensive literature survey and identification of research gap
   b. Structuring of research paper / patent document
   c. Technical depth, methodology, and clarity of presentation
   d. Patentability analysis (in case of patent track)

   Component 2: Submission / Filing
   a. Submission of manuscript to a reputed Scopus / SCI /WoS indexed journal
   OR
   Filing of a patent application with appropriate authority
   b. Submission proof (acknowledgement / application number) is mandatory

   Component 3: Publication / Patent Outcome
   Publication of article in Scopus / SCI / WoS indexed journal
   OR

Publication of patent

4. Marks shall be awarded proportionately based on:
   a. Paper publication status (accepted / published)
   b. Patent filing / publication status

5. Students must ensure originality and adherence to ethical practices, including proper citation and avoidance of plagiarism.

6. A plagiarism report shall be submitted, with similarity generally not exceeding 10%, failing which revision and resubmission is required.

7. Progress shall be monitored through periodic reviews by the departmental committee, focusing on:
   a. Conversion of project work into quality manuscript / patent
   b. Quality of manuscript / patent drafting
   c. Readiness for submission / publication

8. The HOD shall constitute publication/patenting evaluation/review committee(s) & the composition shall be as follows:
   a. HOD or one of the HODs in case of an interdisciplinary project, shall be the Chairman of the committee
   b. Coordinator shall be member - Convener
   c. Guide shall be the member
   d. One/Two senior faculty members nominated by the HOD (may be from different departments in case of an interdisciplinary project jointly nominated by the HODs)

Deliverables:

1. Literature Review Report / Patentability Report
   a. Representation of problem identification
   b. Representation of gap analysis
   c. Survey of recent literature / prior art

2. Manuscript / Patent Draft
   Structured manuscript (Abstract, Introduction, Methodology, Results, References)
   OR
   Patent Draft (Title, Abstract, Claims, Description, Drawings)

3. Submission Proof
   Journal submission acknowledgement / Patent filing receipt

4. Paper Publication / Patent Filing / Patent Publication Evidence

Evaluation for CIE:

Total of 100 CIE marks is distributed as follows:

Sl. No.	Description	Marks
1.	Literature Review, Research Paper Writing / Patentability Search, Drafting the Patent Application	50
2.	a. Submission & Acceptance of manuscript (Scopus / SCI / WoS) OR b. Filing a Patent Application	30
3.	a. Publication of Article (Scopus / SCI / WoS) OR b. Publication of Patent	20
	Total	**100**

Course Outcomes:

At the end of the course, the student will be able to:

1. Systematically document literature review and gaps in a specific domain
2. Prepare a structured research manuscript or patent document following standard guidelines
3. Perform patentability search and analyze prior art for innovation feasibility
4. Demonstrate the ability to submit research work to journals or file patent applications
5. Apply ethical practices in research, including plagiarism avoidance and proper citation